Boylested
SM Wasko Ch4

23/9/19

Device and circuit: Diode, BJT

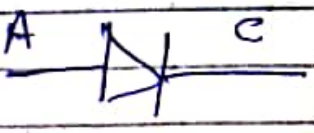
Devices.

connect devices properly to get a circuit.

Construction
characteristics
Application.

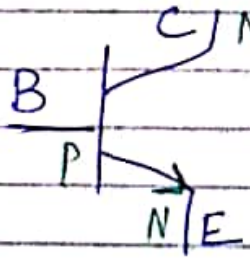
diode → rectifier

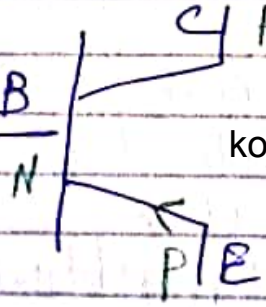
Arrow pointing from P to N.



Two types of BJT transistors.
NPN and PNP.

bipolar → the conduction is due to both electrons and holes.



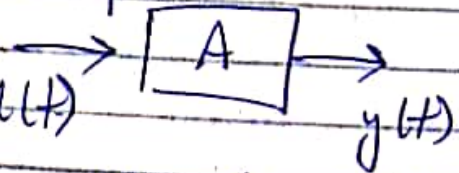


Arrow is always on the emitter terminal and pointing from P to N.

Two main applications.

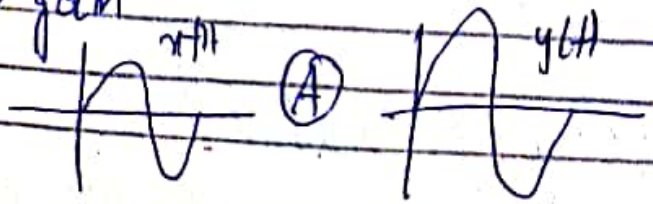
Amplification

Switching



$y(t) = A\,x(t)$

A → gain



Amplifier doesn't change the frequency.
It changes amplitude and power

Same start and end point → same phase

The amplifier that produces 180° phase shift b/w input and output is called inverting amplifier. → voltage gain is negative

↳ common emitter, base, collector

phase shift 180° 0° phase shift

Three regions in the characteristics of BJT.

(i) Linear → for amplification
(ii) Saturation → for switching
(iii) Cut off
(iv) Breakdown. → damage

KVL → $\Sigma V = 0$ KCL → $\Sigma I = 0$

Capacitor:

(i) Non polarized or static capacitor ⊣⊢
↳ can be connected to any polarity in any way.

(ii) Polarized ⊣⊢

Battery cell ⊣⊢

Battery → many battery cells combined ⊣⊢⊣⊢

FIELD EFFECT TRANSISTOR (FET)

signal → something carrying information and depends on an independent variable.

varying with time → analog signal
we have a value of that signal at any instant of time

Analog Amplifier

- Rectifier
- Amplifier
- Oscillator

Transistor

- BJT
  - NPN
  - PNP
- FET
  - Junction FET
    - n channel JFET
    - p channel JFET
  - MOSFET metal oxide semiconductor FET
    - Depletion type
      - n channel
      - p channel
    - Enhancement type
      - n
      - p
  - MESFET metal semiconductor FET

data structures

tree

top → root
bottom → leaves

FET like BJT → 3 terminal device

Gate ⟷ Base controlling terminal
Drain ⟷ Collector
Source ⟷ Emitter

FET → voltage controlled device
BJT → current controlled device
↳ Base current controls collector current

↳ Gate to source voltage (V_{GS}) controls the drain current.

FET → unipolar → current is either due to electrons or holes. (1 type of carrier)
BJT → bipolar → current is due to both type of carriers

Input impedence of FET is higher than BJT.
Voltage gain of BJT is high than FET

FETs are smaller in size.
↳ nowadays ICs with FETs → MOSFET
↳ packing density is very high

FETs are thermally stable.
FET Require less power ($P=I^2R$ loss)

Construction

n channel JFET

conduction due to electrons

Gate (G)

Terminals

Drain and

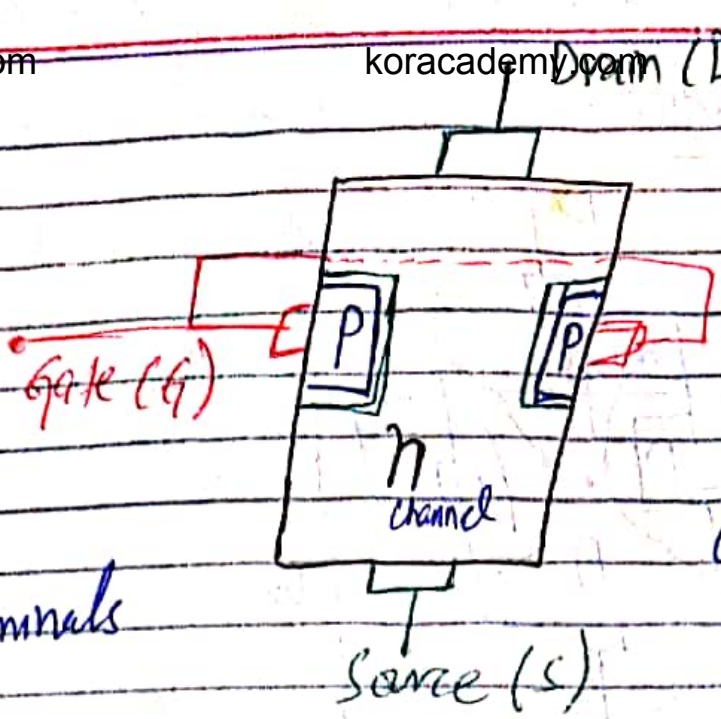
Two PN

B/w Gate
a junction

junction

For p chan

G



Ohmic contacts.

Terminals

Drain and source can be interchangably used.

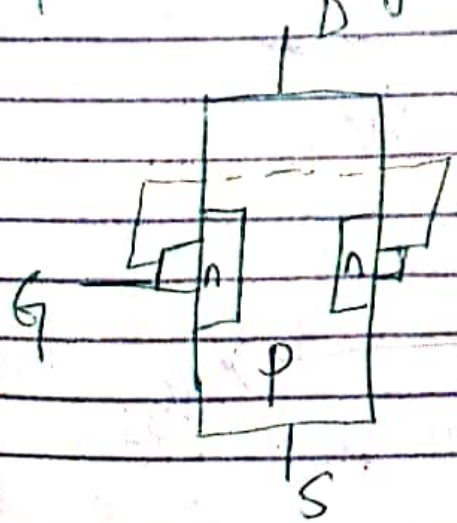
Two PN junctions have been formed.

Blw gate and ~~terminal~~ channel there is a junction → therefore ~~FET~~ junction FET.

junction is there → depletion region will be there.

↳ no free charge carriers developed due to diffusion.

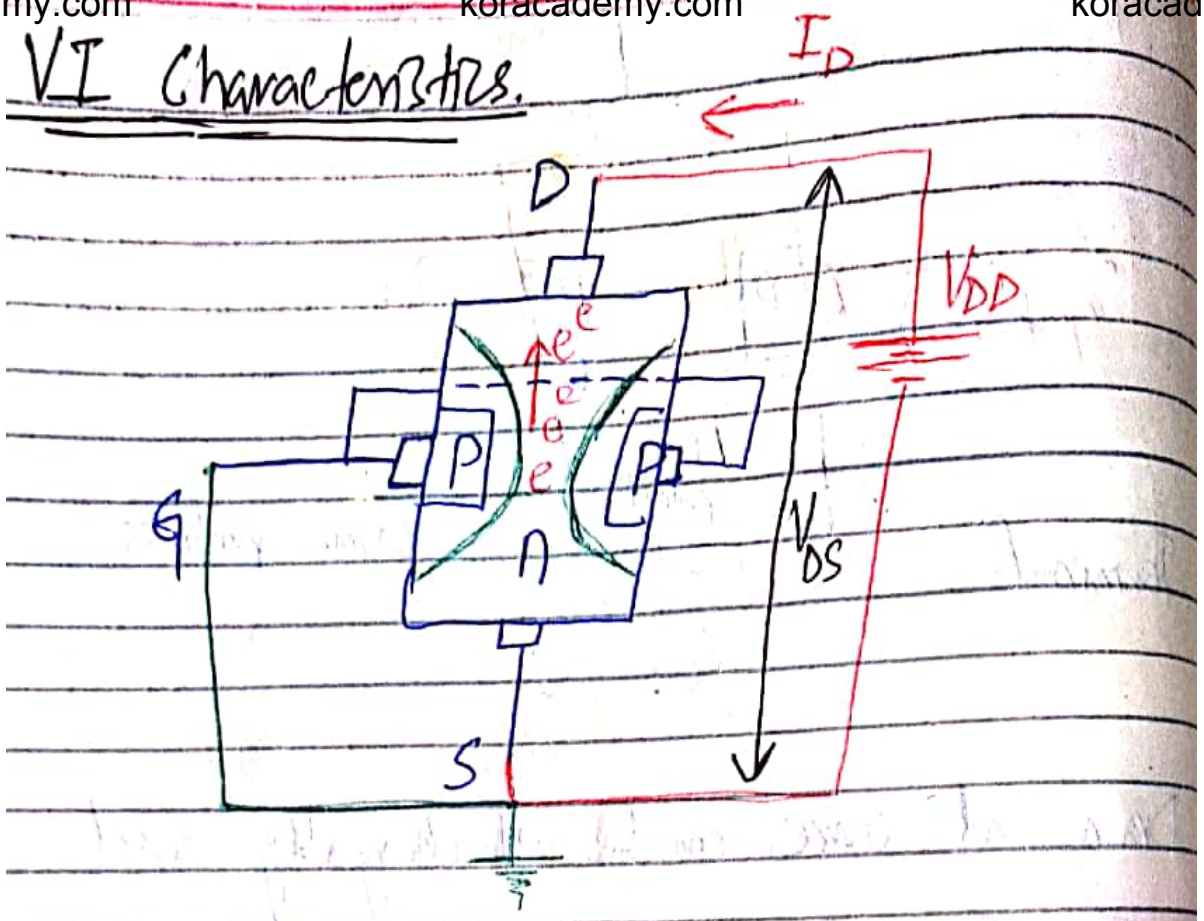
For p channel → gate is n and channel is p.



Gate is controlling the current b/w drain and source.

FET → voltage controls current.
BJT → current controls current.

VI Characteristics.

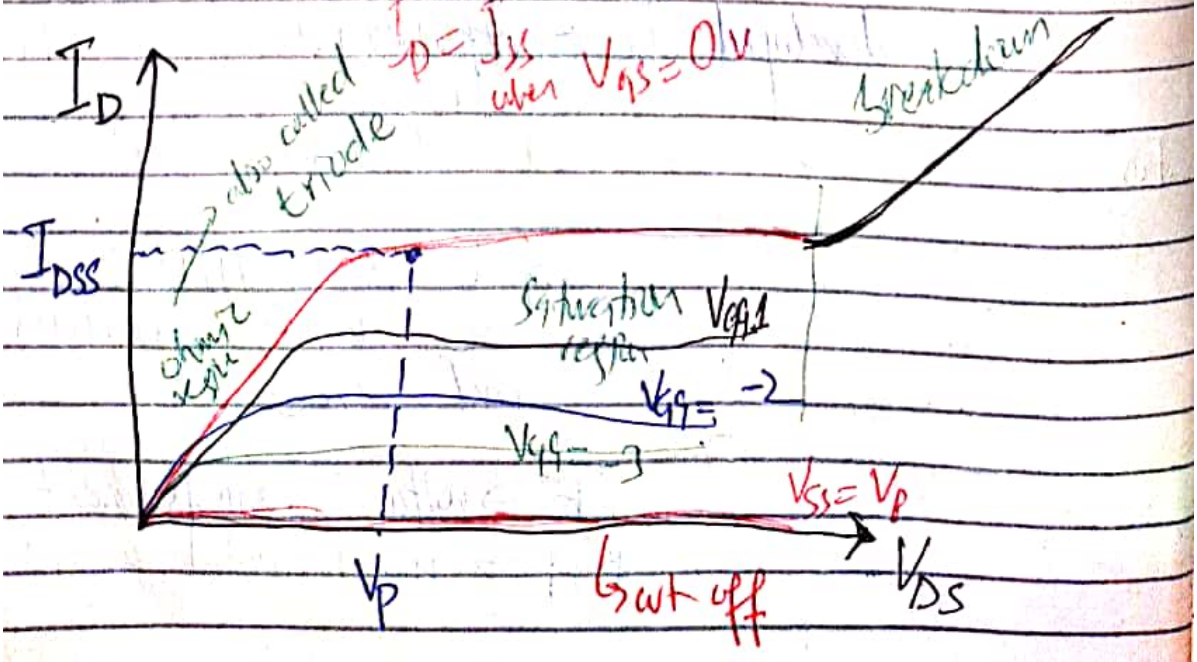


$V_{GS} = 0$

voltage symbol (V) with double small subscript is supply voltage.

Single subscript V → voltage from that point to the ground.

Subscripts → capital → DC
→ small → AC



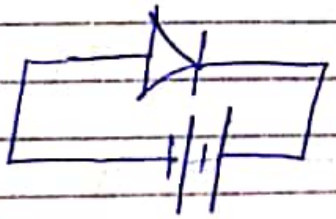
→ I_{DSS}

Current maximum → flat graph → no increase → pinch off voltage → V_p → pinch off

I_{DSS} ⇒ drain current when source is short circuited to current.

Both PN junctions reverse biased → depletion region becomes wider and wider.

Upper part more R.B → d.r wider more in upper part



↳ n has more +ve charge

↳ so the conduction path (channel) becomes thin.

It seems that the two P regions touch each other. → pinch off

Slope of horizontal line = 0 Vertical = ∞.

$\frac{I}{V} = G$ (Conductance) $\frac{V}{I} = R$ $R = \frac{1}{G}$

Further increase voltage → breakdown.

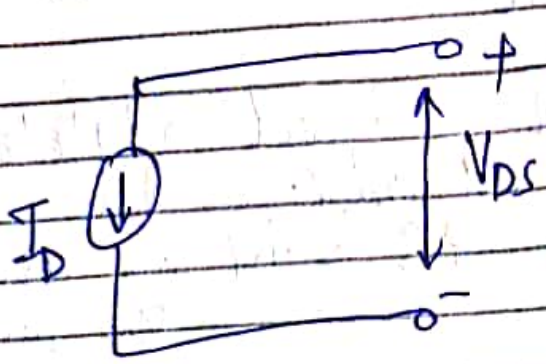
Saturation region (constant current region) is used for amplification

↳ The behaviour of device in this region is like a constant current source.

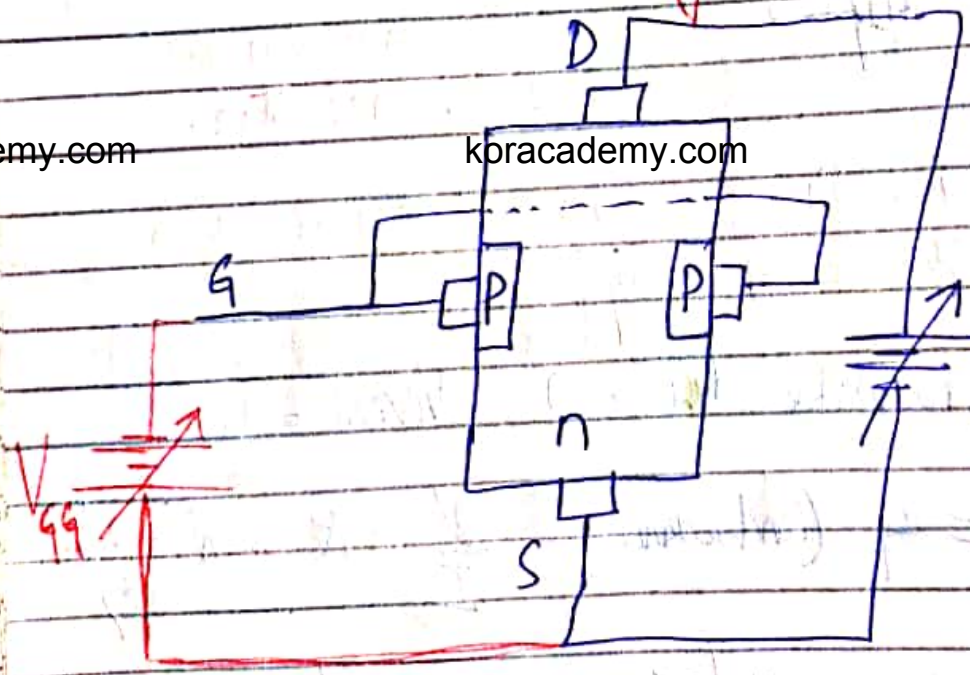
↳ provides current constant irrespective of load

and internal resistance ideally is infinite

Constant voltage source → provides constant voltage irrespective of the load and internal resistance is ideally zero.



PN junction will always be reverse biased.



pinch off will now occur earlier by applying V_{GG}.

When $V_{GS} = V_P$ → $I_D = 0$ → channel off → cut off mode

V_{GS} → input voltage V_{DS} → output voltage
I_D → output current

These characteristics are called drain characteristics.
I_D Vs V_{DS} for given V_{GS} value.

I_C Vs V_{CE} for given value of I_B → collector characteristics
↳ spacing is uniform → so linear relationship between I_C and I_B $I_C = \beta . I_B$

↳ spacing b/w curves is not uniform.
↳ so non linear relationship.

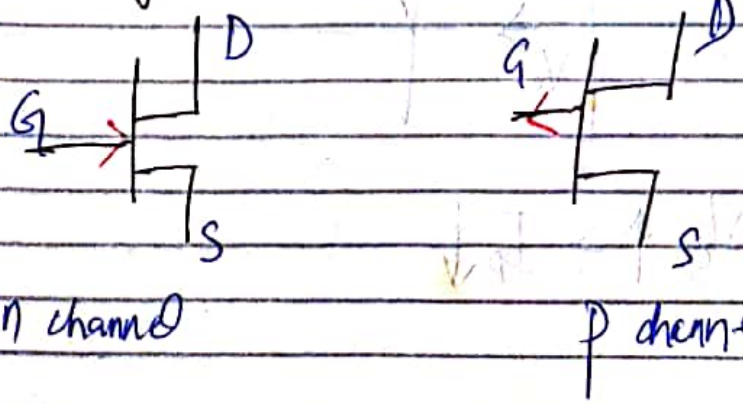
Transfer Characteristics:

transfer → involvement of both input and o/p parameters

For n channel V_p is negative.
On the datasheet of a device it is given as V_{GS} off.

$I_D = 0$ | $V_{GS} = V_p$ $\quad$ $I_D = I_{DSS}$ | $V_{GS} = 0$

JFET symbol



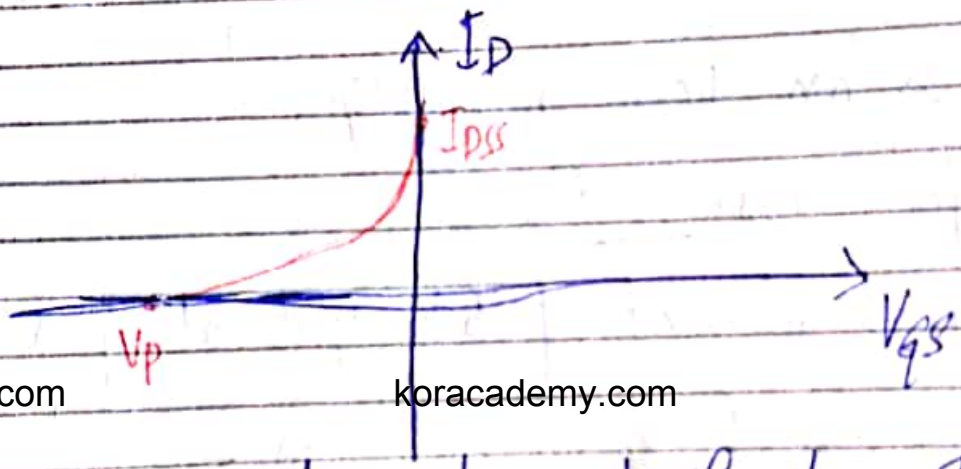
Transfer Ktns By Shockley

I_D Vs V_{GS} plot for a given value of V_{DS}

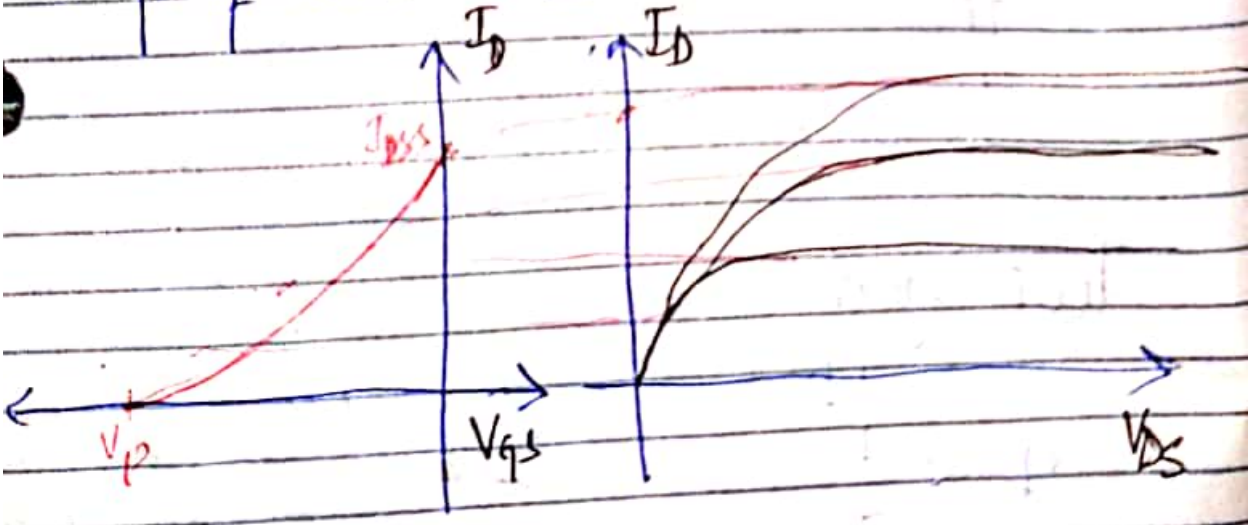
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

I_{DSS}, V_P → constants I_D → controlled variable

V_{GS} and V_P should have the same polarity



② We can also draw transfer chs with the help of drain characteristics



$V_{GS}\uparrow \rightarrow I_D\downarrow$

Short Hand Method:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

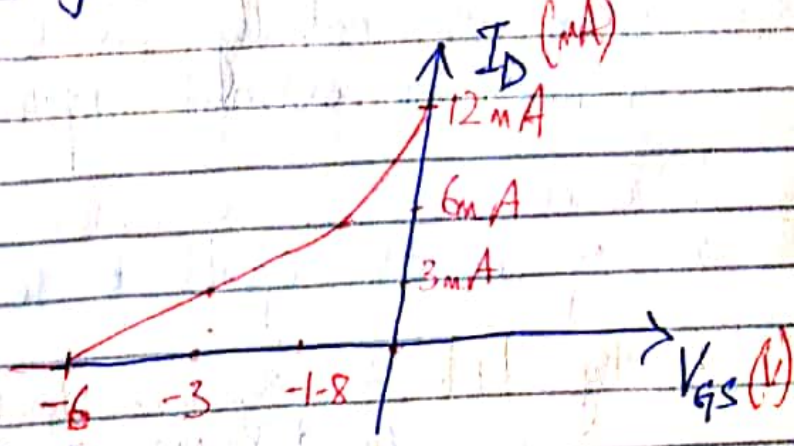
or $$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0

Example Sketch the transfer curve for the device where $I_{DSS} = 12\ mA$ and $V_P = -6\ V$

n channel JFET

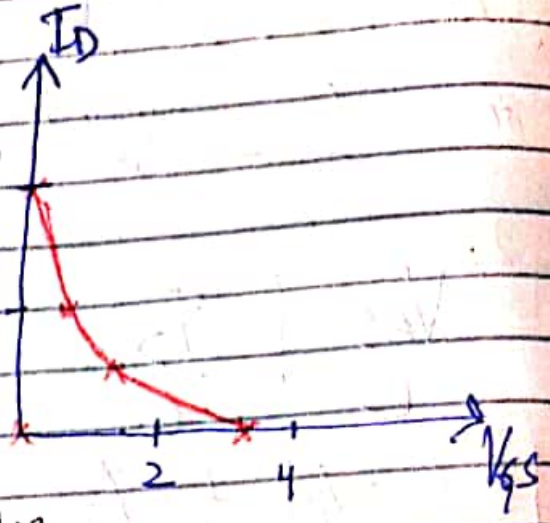
V_{GS}	I_D
0	12 mA
-1.8V	6mA
-3V	3mA
-6	0



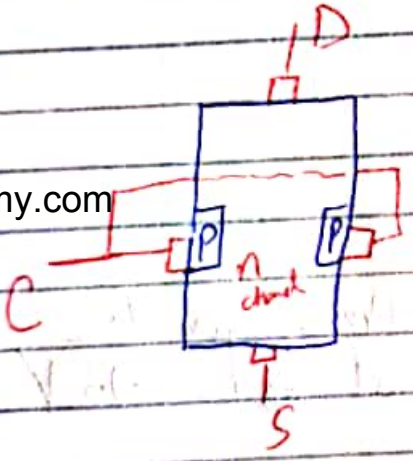
Example $I_{DSS} = 4mA$ $V_p = 3V$

V_p = +ve ⇒ p channel

V_{GS}	I_D
0	4 mA
0.9	2mA
0.15	1mA
3	0



Lecture 2 30/9/19



Take silicon w

silicon → 4 valence electrons

when silicon with pentavelent

→ 4 bonds → ~~to Sonded~~

Hole → defficency of electrons

Intrinsic → purest form of semiconductor which is naturally available

Extrinsic ⇒ external impurity is added

Overall the structure remains neutral → total no. of electrons equals to the total no. of neutrons

Why depletion region is developed?

Due to diffusion → Current flows from higher concentration to lower

one side majority electrons → one side holes

Depletion region consist of no free charge carriers.

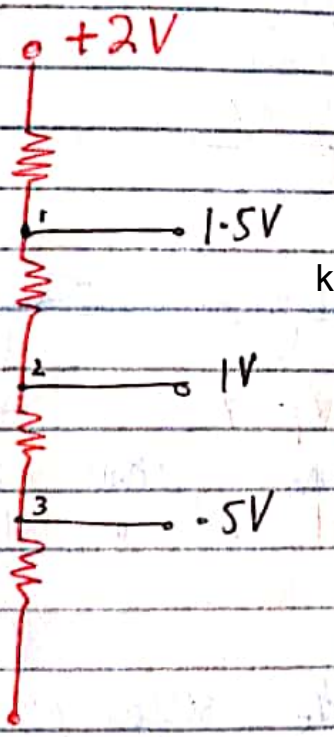
Two PN junctions and therefore two depletion regions.

↳ D.R is uniformly produced → Now connect biasing voltage → so drift current will flow.

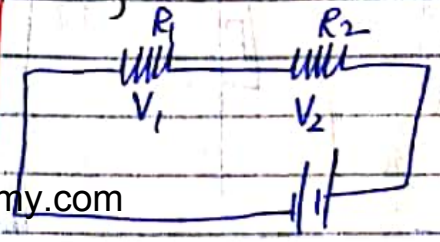
↳ depletion region widens.

$I_D = I_{DSS}\Big|_{V_{GS}=0V}$ $\quad V_{DS} \geq V_p$

How depletion region develops?



voltage divider rule?



↳ applicable to series resistance.

$V_1 = \left(\frac{R_1}{R_1+R_2}\right)V$

Similarly $V_2 = \left(\frac{R_2}{R_1+R_2}\right)V$

can be applied to any no. of devices connected in series.

Current divider rule?

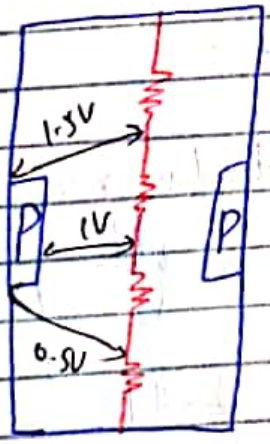
Applicable to parallel connections.

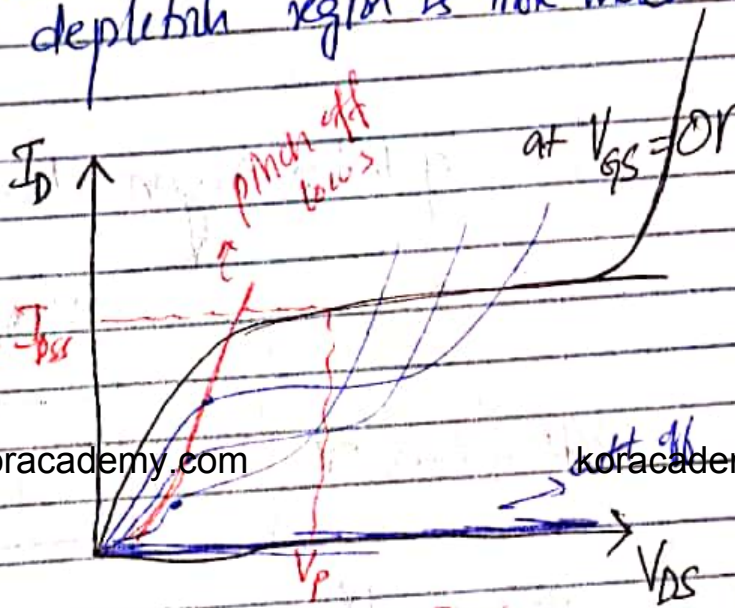
opposite current is taken.

$$I_1 = \left(\frac{R_2}{R_1+R_2}\right) I \qquad I_2 = \left(\frac{R_1}{R_1+R_2}\right) I$$

Current divider rule is applicable to only two devices connected in parallel.

Upper portion → more potential → more reverse biased → depletion region is more wider



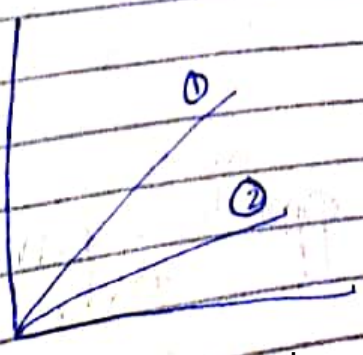


o/p ch or dram ch → 4 regions

cut off | breakdown | Saturation (used for amplification) | ohmic

For n channel we apply negative V_{GS}.

With application of V_{GS}, the slope increases → result is the increase in ~~resistivity~~ conductivity.



$$G_1 = \frac{I_1}{V_1}, \quad G_2 = \frac{I_2}{V_2}$$

$$G_1 > G_2$$

$$R_1 < R_2$$

pinch off will occur earlier.

When V_{GS} becomes more and more negative, slope decreases → increased resistance

When we join VP points in the chs, we get locus of pinch off value.

Ohmic region is also called voltage controlled resistance region.

JFET acts as a variable resistor in this ohmic region.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

→ Resistance in the ohmic region.

r_o → channel resistance when $V_{GS} = 0V$

r_d → for any value of V_{GS}.

Example For n channel JFET, $r_o = 10K\Omega$ where $V_{GS} = 0V$ and $V_P = -6V$. Determine the channel resistance when $V_{GS} = -3V$

$r_d = ?$ $\quad r_d = \frac{10 \times 10^3}{\left(1 - \frac{(-3)}{(-6)}\right)^2}$ $\quad (1/2)^2 = 1/4$

$\Rightarrow r_d = 40 \times 10^3 \Omega \Rightarrow 40 K\Omega$

At $V_{GS} = -4V$

$$r_d = \frac{10K}{\left(1 - \frac{(-4)}{(-6)}\right)^2} = \frac{10K}{\left(1 - \frac{2}{3}\right)^2} = \frac{10K}{1/9}$$

$\Rightarrow 90 K\Omega$

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

Two types of MOSFET
① Depletion type MOSFET → n / p
② Enhancement type MOSFET → n / p

MOSFET is a subclass of FET.

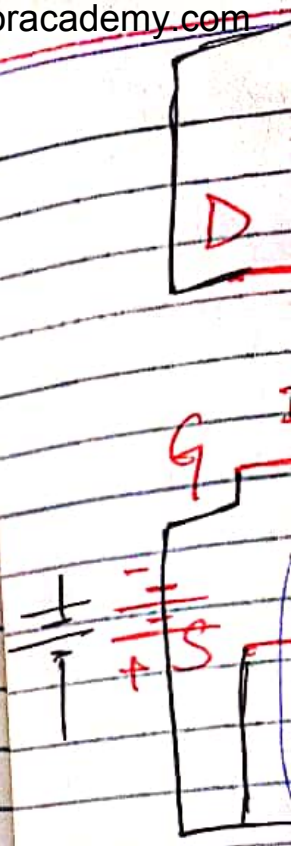
Its operation is very similar to JFET.
From cut off to saturation and I_{DSS}, they are similar.

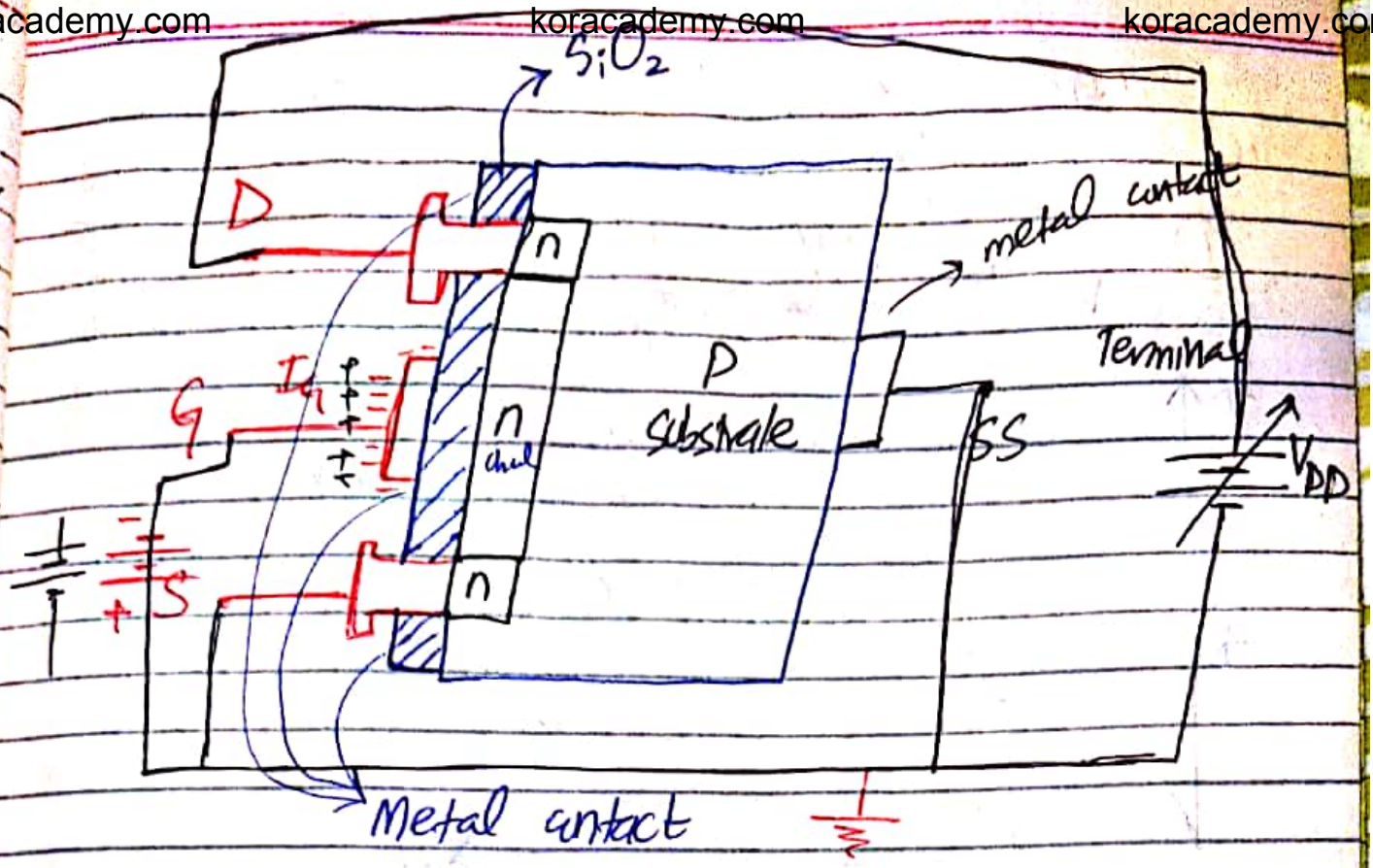
What additional in MOSFET?
The current can flow beyond I_{DSS}
↳ meaning that I_{DSS} is not the maximum current here

Construction:
Take si base and form p type substrait (base)
↳ n

n channel Depletion type MOSFET

substrait is p type and the channel is n type.
Substrate provide the foundation on which the device is made
channel physically exists





n → heavily doped n materials. → more free
n (in some books n^+) charge carriers
are there to increase conductivity.

Gate is metal.

B/w Gate and channels SiO_2 layer.

4 terminals.

Sometimes the source terminal is connected to substrate → 3 terminal device

Connect the power supply?

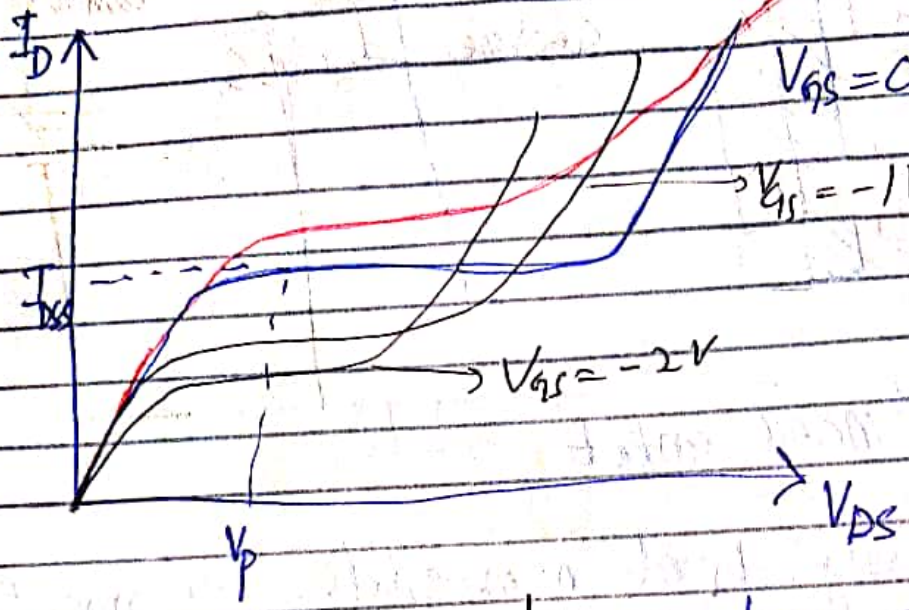
B/C of the presence of SiO_2 layer (dielectric), the input resistance of DMOSFET is very high

$V_{GS} = V_{GSS}$

natural current and electron current have the same direction.

① $V_{GS} = 0V$

$I_D = I_{DSS}$ $V_{DS} \geq V_p$



In depletion mode we have to deplete the channel of free charge carriers.

Similar charges repel each other.
opposite " attract "

② we apply -ve V_{GS}. $V_{GS} < 0$ $V_{DS} \geq 0$
↳ electrons → repell
↳ so the current reduces
↳ active device → we control the current.

In case of JFET, we cannot apply the voltage

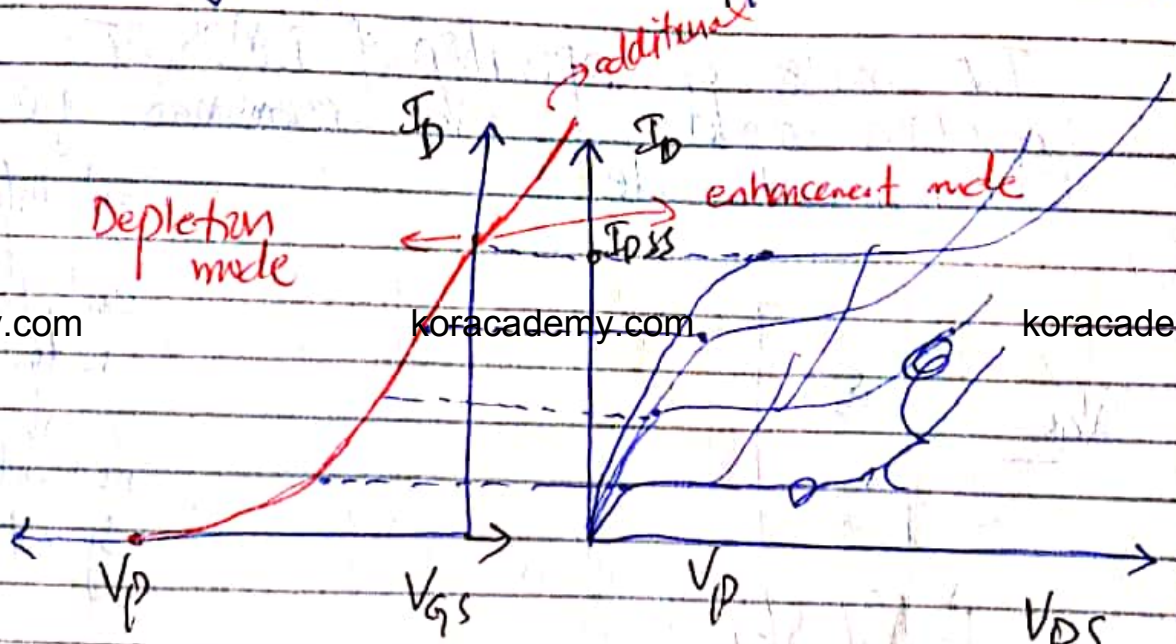
(3) Apply +ve V_{GS} $V_{GS} > 0$ $V_{DS} \geq V_p$

Now the operation would be just like capacitor.

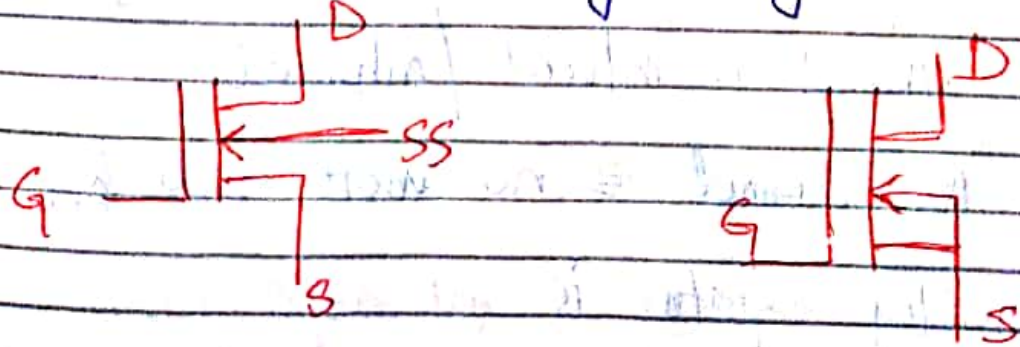
Electrons from p substrate will be attracted towards the channel

↳ density of carriers increases → current increases.

Shockley equation is also applicable to DMOSFET.

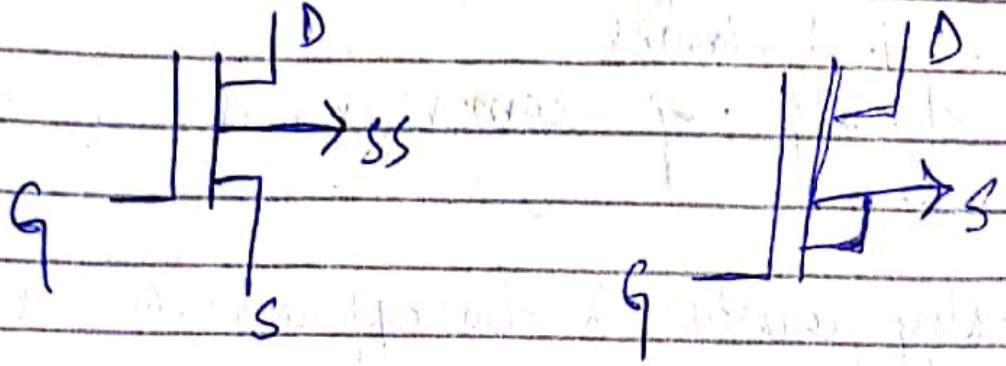


n channel D MOSFET symbolically

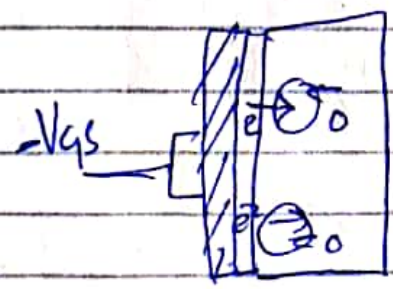


Gap b/w Gate and channel?
Shows there is no electrical connection b/w them.

P channel DMOSFET.



Two modes of operation of DMOSFET;
Depletion mode
Enhancement mode



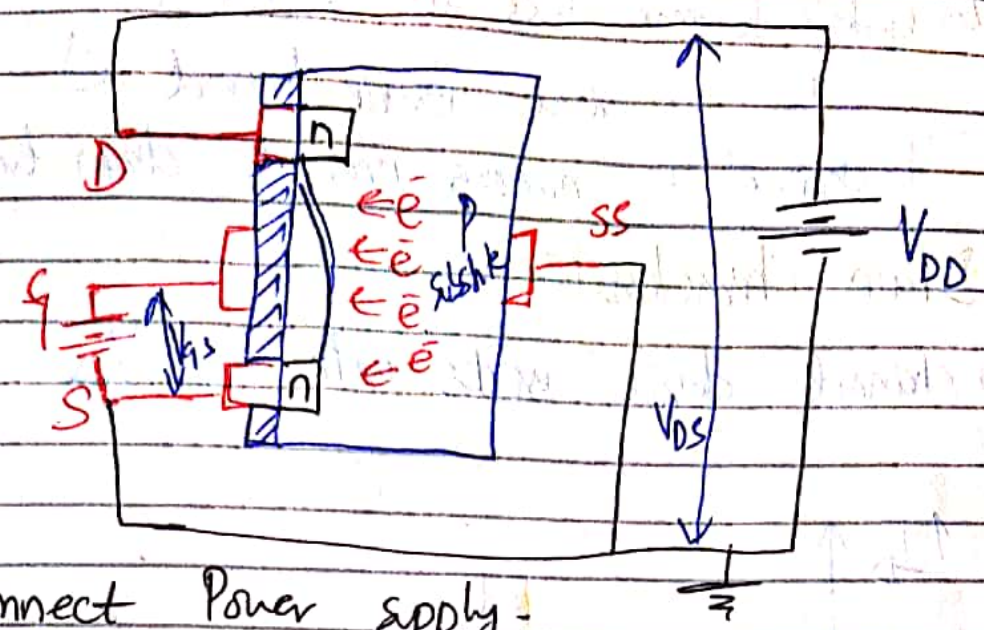
EMOSFET

There is no channel in the beginning.
The channel is induced / enhanced.
No channel ⇒ no current ⇒ no I_{DSS}.
Shockley equation is not applicable

, -Vgs, recombination of e and holes
↓
conductivity reduced
↓
current controlled by voltage

n channel E MOSFET:

JFET operates only in depletion mode



Connect Power supply.

Two PN junctions

+ve V_{GS} will be applied
↳ initially no current → when increased to a particular threshold value → current (drain current) starts flowing.

↳ electrons will be attracted from p substrate. SiO_2 layer is acting as n channel and current starts flowing.

No I_{DSS} s/c no channel exists.

EMOSFET operates only in enhancement mode.

Depletion region is also formed.

Applying KVL; $-V_{DG} - V_{GS} + V_{DS} = 0$

or $V_{DG} + V_{GS} - V_{DS} = 0$

$V_{DG} = V_{DS} - V_{GS}$

$V_{GS} = 8V$ and V_{DS} increases from 2 to 5V

$V_{DD} = ?$ will vary from -6 to -2 V

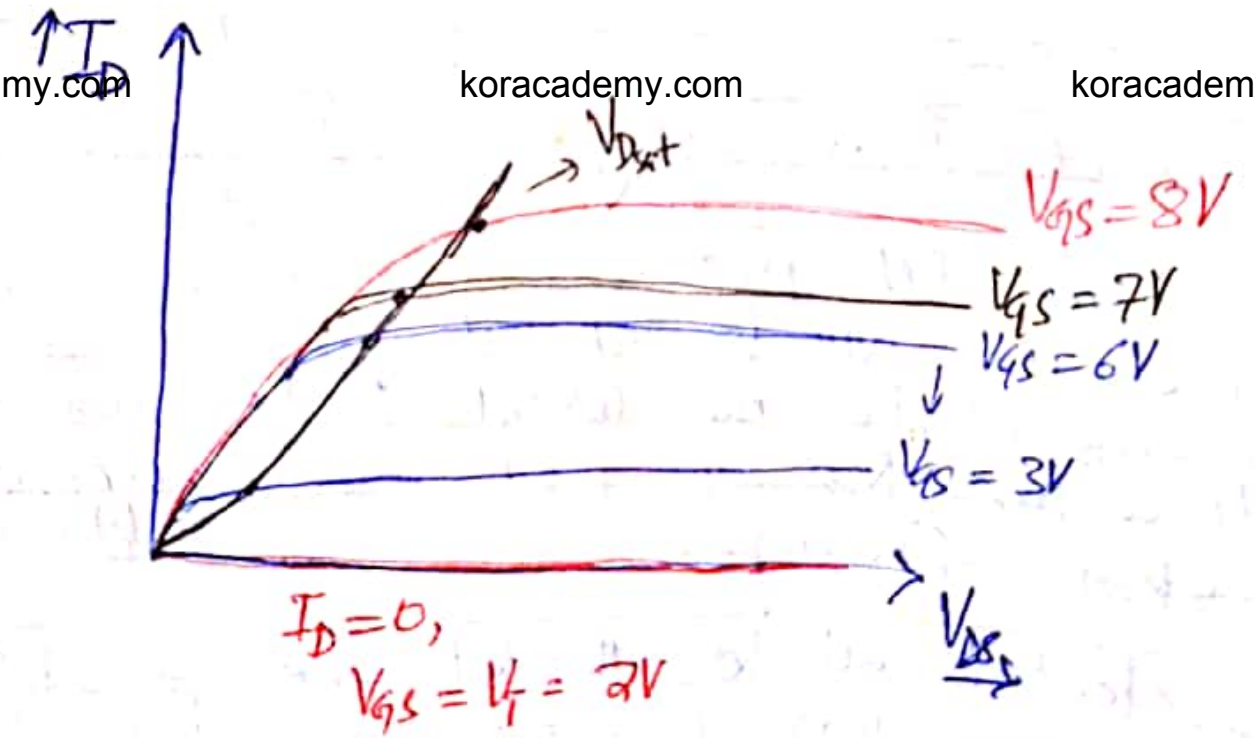
↳ Gate become less +ve w.r.t drain.

↳ is more reverse biased ↲

↳ channel is narrow near the drain terminal.

Dram Characteristics

n channel depletion works with +ve V_{GS}

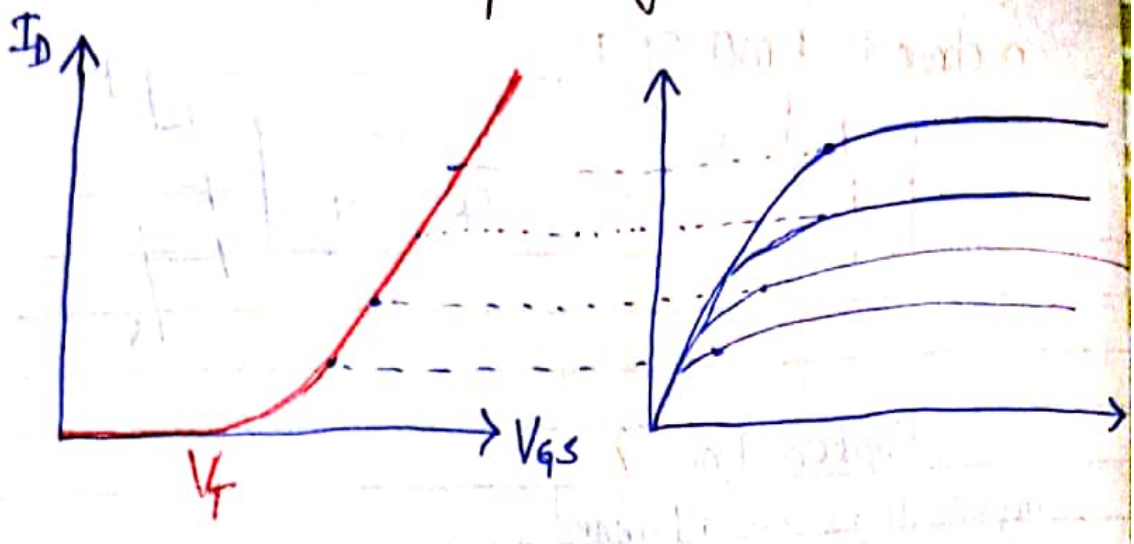


V_t → threshold voltage mentioned in the data sheet as $V_{GS(th)}$

Locus → locus of V_{DS} saturation.

Transfer characteristics:

I_D vs V_{GS} plot for a given value of V_{DS}.



$$V_{DS_{sat}} = V_{GS} - V_T$$

for $V_{GS} \leq V_T$ $\quad I_D = 0$

for $V_{GS} > V_T$ Drain current exists.

Relationship b/w I_D and V_{GS};

$$I_D = K (V_{GS} - V_T)^2$$

K → constant → depend on construction of device

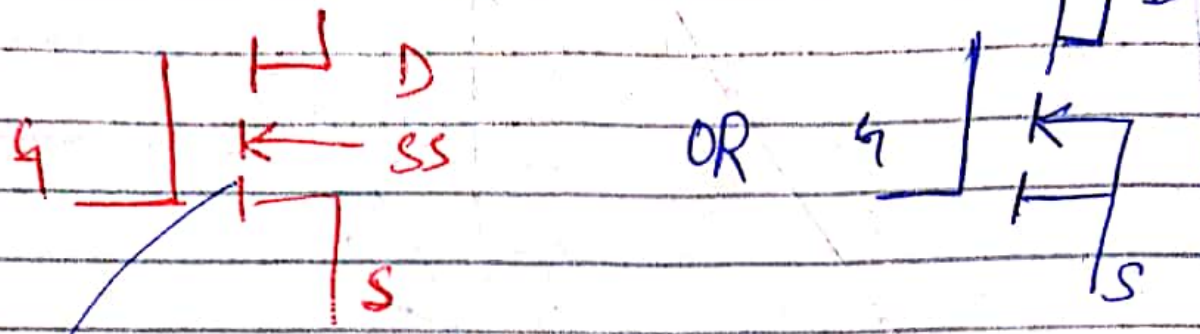
$$K = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$ Unit A/V^2

let $I_{D(ON)} = 10mA$ $\quad V_{GS(ON)} = 8V$ $\quad V_T = 2V$

$K = ?$ $\quad K = \frac{10m}{(6)^2}$

Symbols

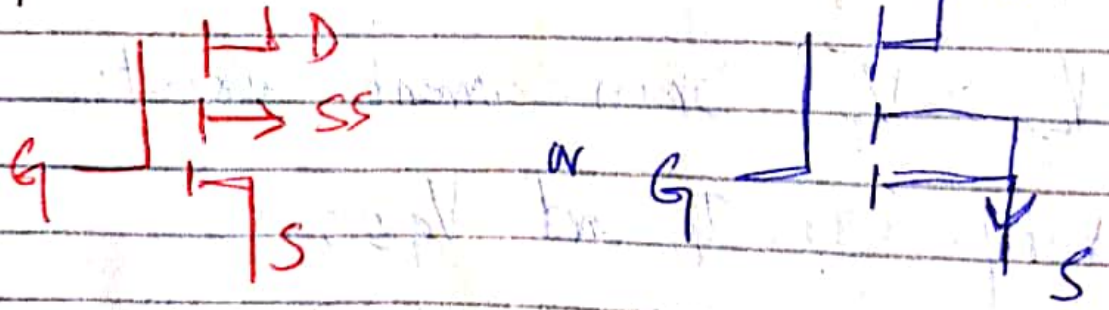
n channel EMOSFET



Broken line ?

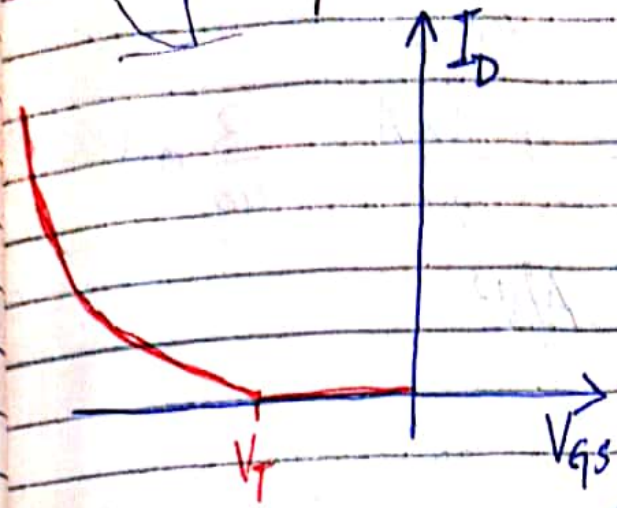
Physically no channel exists b/w D and S

P channel EMOSFET



Drain characteristics.

Transfor characteristics (p channel EMOSFET)

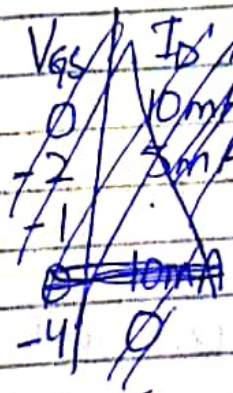


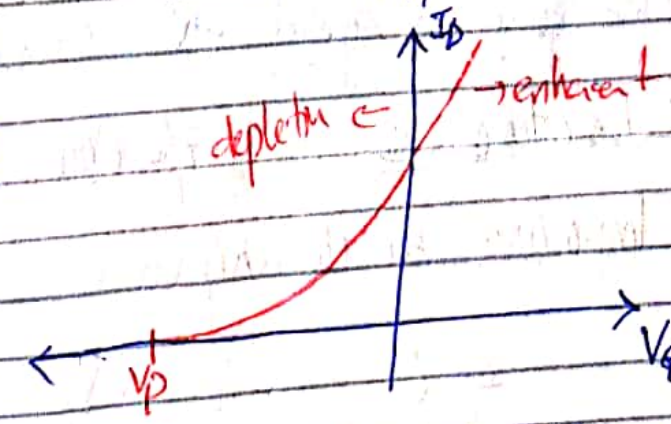
Example: Sketch the transfer ch of depletion type MOSFET $I_{DSS} = 10mA$ | $V_p = -4V$ → n channel

V_{GS}	I_D
$0.3V_p$	$I_{DSS}/2$
$V_p/2$	$I_{DSS}/4$
V_p	0
0	I_{DSS}

V_{GS}	I_D
0	10mA
-2	2.1
$-V_p$	0

[+ve] →





Increase V_{GS} in the direction → current increases beyond I_{DSS}

K=? plot Transfer ch → n chnl Enhmt

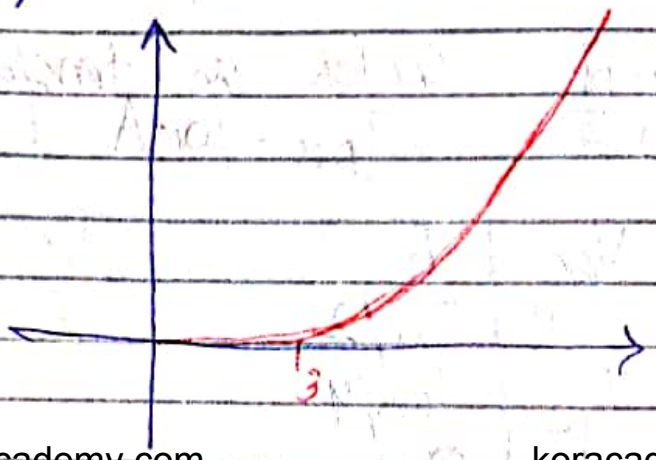
$V_t = 3V$ $I_{D(ON)} = 3mA$ $V_{GS(ON)} = 10V$

$$K = \frac{3mA}{(10-3)^2} = \frac{3mA}{7^2} = \frac{3}{49}mA$$

$$K = 0.061 \times 10^{-3} A/V^2$$

$$I_D = K(V_{GS} - V_t)^2$$

V_{GS}	I_D
~~0~~	
~~3~~	→ 0
~~5~~	→
6	→
7	→

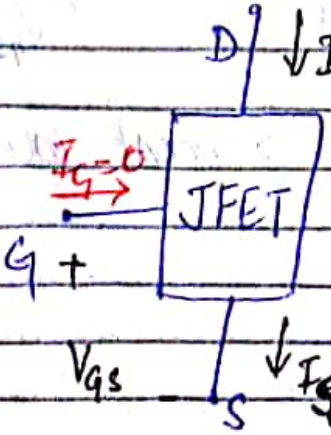


square meter → unit of area

meter square → square with each side of 1m

Lecture 3 07/Oct/19

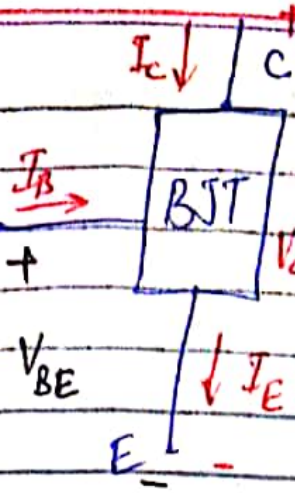
Importon Relationships.



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$I_G = 0$ $I_D = I_S$

voltage controlled device.



$I_C = \beta I_B$

$V_{BE} = 0.7\,V$

$I_C \cong I_E$

Current controlled device.

For n channel, V_p is negative and for p channel it is positive.

In MOSFET, gate is metal and is separated from channel by silicon dioxide layer.

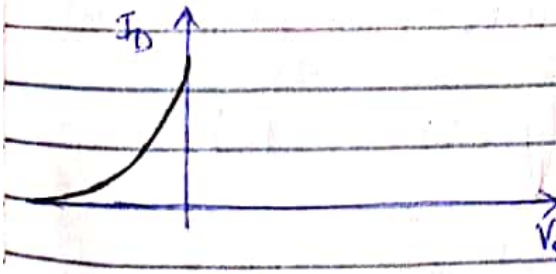
In JFET, the gate and channel are seperated by a PN junction.

In DMOSFET, physically channel exits.

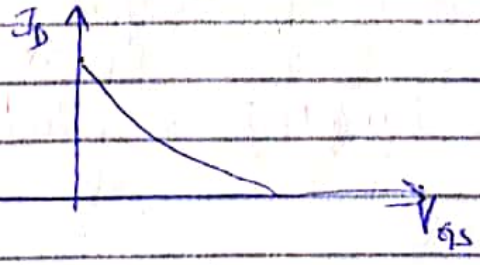
In EMOSFET, channel doesn't physically exist; it is induced / enhanced → inversion layer.

n type material is introduced artificially.

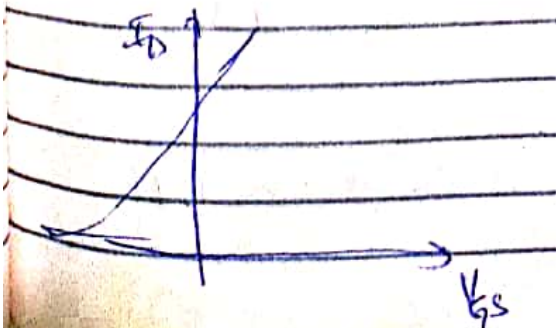
n channel JFET



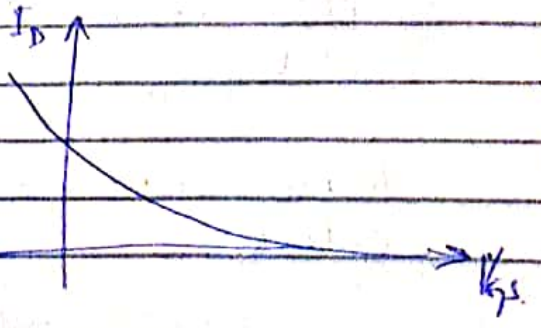
p channel JFET



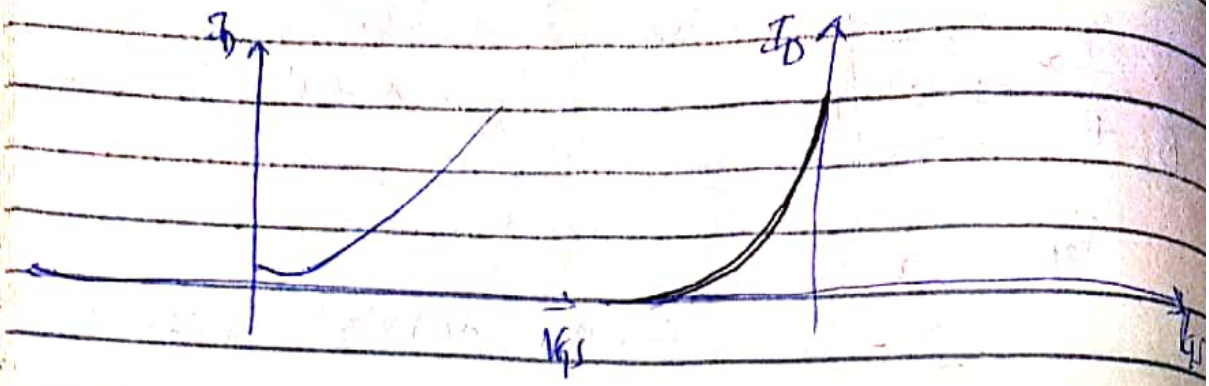
n channel DMOSFET



p channel DMOSFET



n channel EMOSFET p channel EMOSFET



Transfer ch y/c it involves both i/p and o/p quantities. (I_D vs V_{GS} plot).

MOSFETs are also called insulated gate FET ie IGFET.

One plate second plate → separated by dielectric → capactive phenomena (gate and channel)

Curve tracer → oscillascope like device to study drain ch of FET or collector ch of BJT.

DMOSFET is also called normally ON device. If there is no V_{GS} applied, still conduction will take place b/w gate and source.

EMOSFET is called normally OFF device.

↳ $I_D = K(V_{GS} - V_T)^2$

Shockley eq is applicable to JFET, DMOSFET and DMESFET.

Reverse biased d/c anode is more -ve w.r.t cathode

P is more +ve wrt n → it is forward biased.

Silicon dioxide layer is very sensitive and we must protect it → short circuit all the pins of MOSFET (aluminum foil)

While replacing any device practically → the voltage must be off → transient.

Zener protection.

Zener diode is connected in reverse bias in ckt
↳ used for regulation.

6.9 MOSFET Handling-

↳ to avoid transients → ie sudden changes in voltage or current.

In presence of zener diode input impedance will decrease (b/c an easy path is provided b/w G and S)

↳ connected back to back to ~~provide~~ protect from either polarity.

eg 30V zener diode and transient appears b/w G and S, 40V → so 3.d doesn't let go more than 30V → device protected.

Photodiode also works in reverse biased mode.

FET BIASING

DC analysis → to find Q point.
Once Q point is established we provide AC signal to get amplification

BJT → $V_{BE} = 0.7V$ $I_C \cong I_E$ $I_C = \beta I_B$

straight line — AC analysis → to obtain voltage gain

DC Analysis of FET

Two approaches are required to establish Q point;
(i) Mathematical approach
(ii) Graphical approach

Mathematical → square law relationship is linear
Graphical → " " " " non linear.

$[I_G \cong 0 \quad I_D = I_S]$ → all FET applicable

Shockley $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

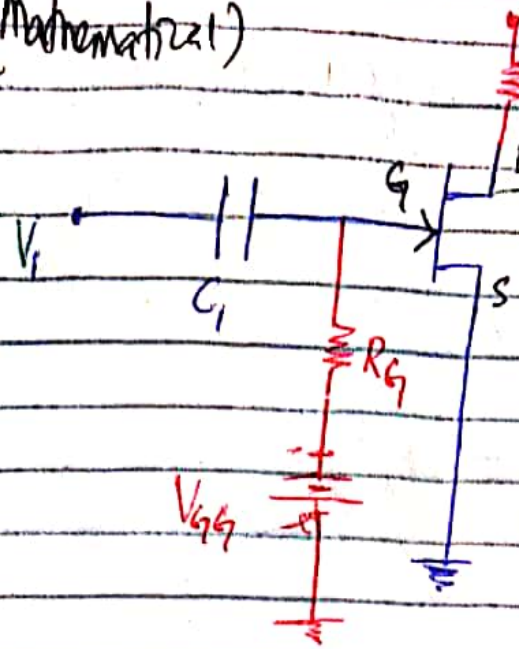
For EMOSFET and EMESFET; $I_D = K(V_{GS} - V_T)^2$

V_{GS} controls I_D
↳ input ↳ output.
↳ control ↳ controlled

Cordinates of Q point = (V_{GS_Q}, I_{D_Q})

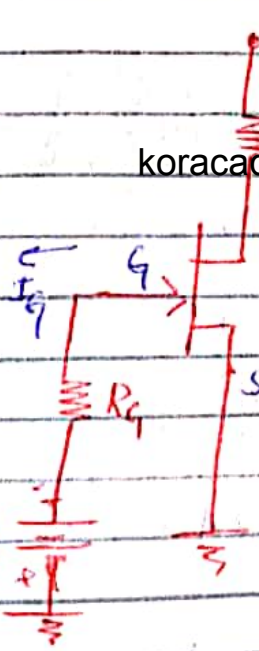
Fixed Bias Configuration (simplest)

(Mathematical)



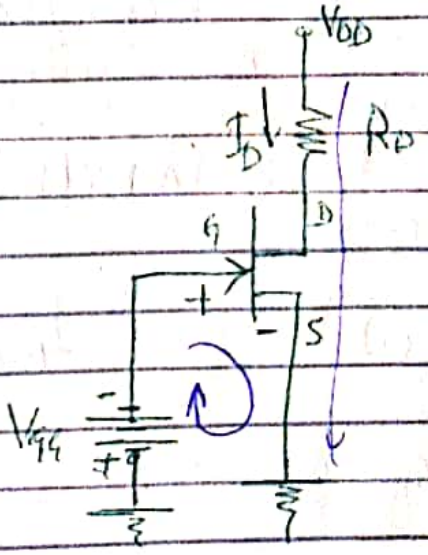
Common source amplifier
(i/p → G o/p → D)

for DC $f = 0$ Hz $\Rightarrow X_C = \frac{1}{2\pi f C} = \infty$



$V_{R_G} = I_G R_G = 0V$

Replace R_G by short circuit equivalent



Apply KVL to i/p loop

$V_{GS} = -V_{GG}$

Gate terminal is always marked with + plus sign

V_{GS} → drop V_{GG} → rise / supply

↳ fixed ⟸ fixed ↵

$V_{GS_Q} = V_{GG}$

↳ Put in shockley eq to get I_{DQ}

KVL to o/p loop

$-V_{DD} + I_D R_D + V_{DS} = 0$

$\Rightarrow V_{DS_Q} = V_{DD} - I_{D_Q} R_D$

Graphical Procedure:

(i) Plot the transfer ch of the device. (I_D vs V_{GS} plot).

(ii) Superimpose the network equation on the transfer ch of the device. (network and line, network and curve)

Network equation results in load line (which is a straight line)

(iii) The intersection of the two curves will give the quissent (Q point).

Device characteristics remain unchanged due to network.

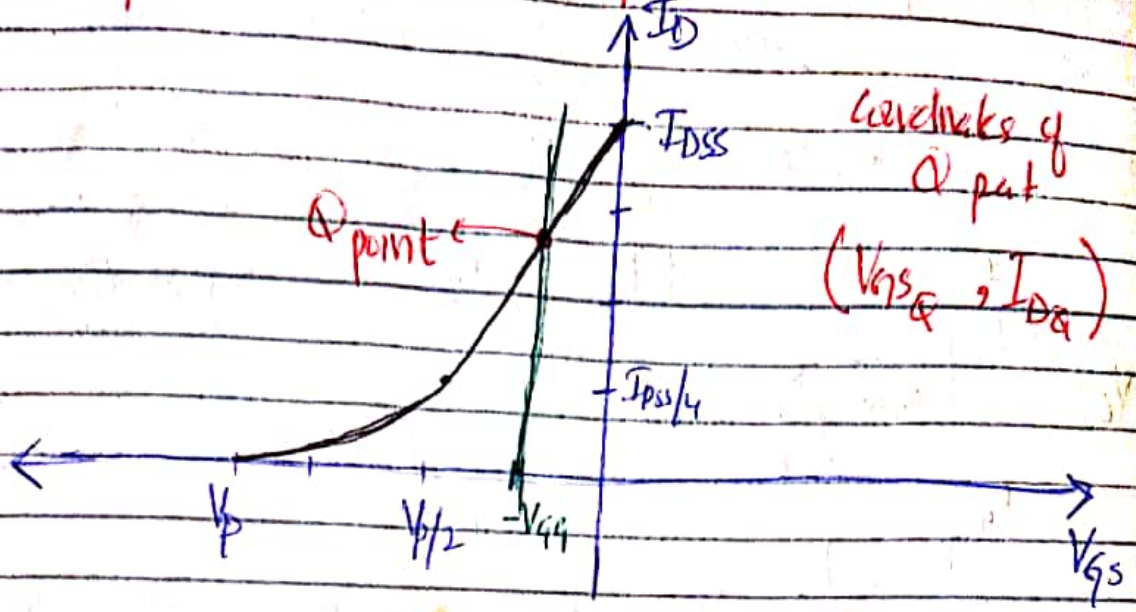
(1) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$V_{GS} = 0$, $I_D = I_{DSS}$ $\quad (0, I_{DSS})$

$V_{GS} = V_P$, $I_D = 0$ $\quad (V_P, 0)$

$V_{GS} = \frac{V_P}{2}$, $I_D = \frac{I_{DSS}}{4}$ $\quad \left(\frac{V_P}{2}, \frac{I_{DSS}}{4}\right)$

Network eq and transfer eq relate the same quantities



$V_{GS} = -V_{GG}$ → network ch.

o/p loop $-V_{DD} + I_D R_D + V_{DS} = 0$

$$V_{DS} = V_{DD} - I_D R_D$$

$V_D = V_{DS} + V_S$ $\quad V_S = 0V$

$$V_D = V_{DS}$$

Limitation.

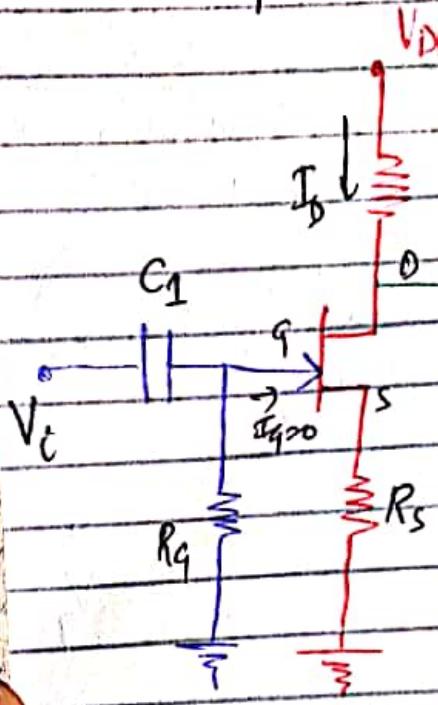
Requires two DC supplies V_{DD} and V_{GS}

Two quantities are provided by the manufacturer I_{DSS} and V_p.

Ex 7.1

Self Biased configuration

common source amplifier

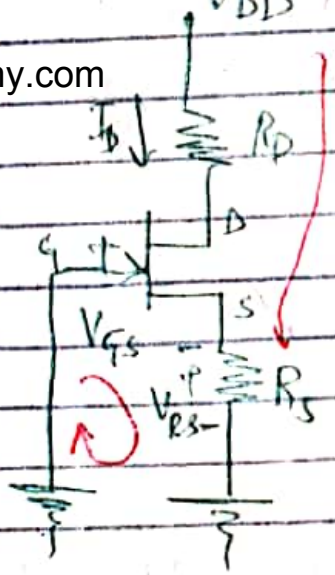


V_{GS} develops due to voltage drop across R_S.

DC → f = 0 → open circuit capacitors

↳ current through $R_G = 0$ so zero voltage drop

↳ short circuit



KVL to i/p loop

$$V_{GS} + V_S = 0$$

network eq ←

$$\boxed{V_{GS} = -I_D R_S}$$

↓

Put this in sh eq

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

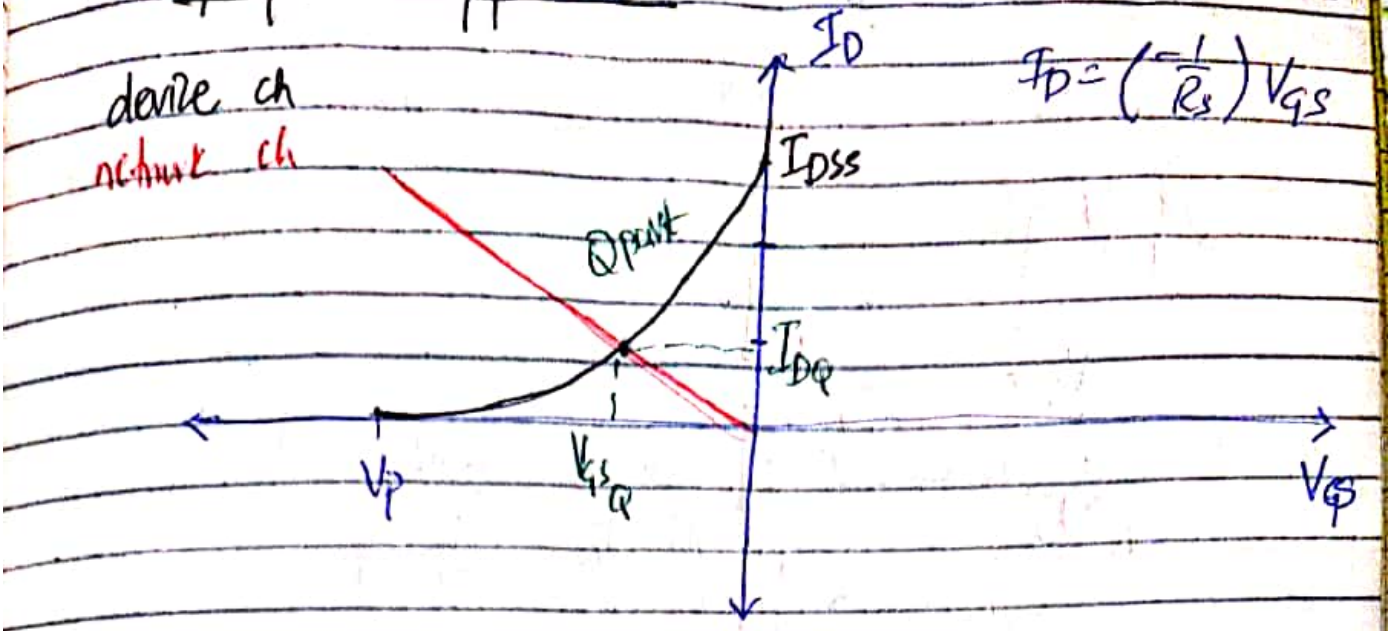
$$I_D^2 + K_1 I_D + K_2 = 0$$

$K_1 = ?$ $K_2 = ?$ assignment

Graphical approach:

$V_{GS} = -I_D R_S$

$I_D = \left(\frac{-1}{R_S}\right) V_{GS}$



KVL to o/p loop.

$-V_{DD} + I_D R_D + V_{DS} + V_{RS} = 0$

$V_{RS} = I_S R_S$, $I_S = I_D$

$-V_{DD} + I_D R_D + V_{DS} + I_D R_S = 0$

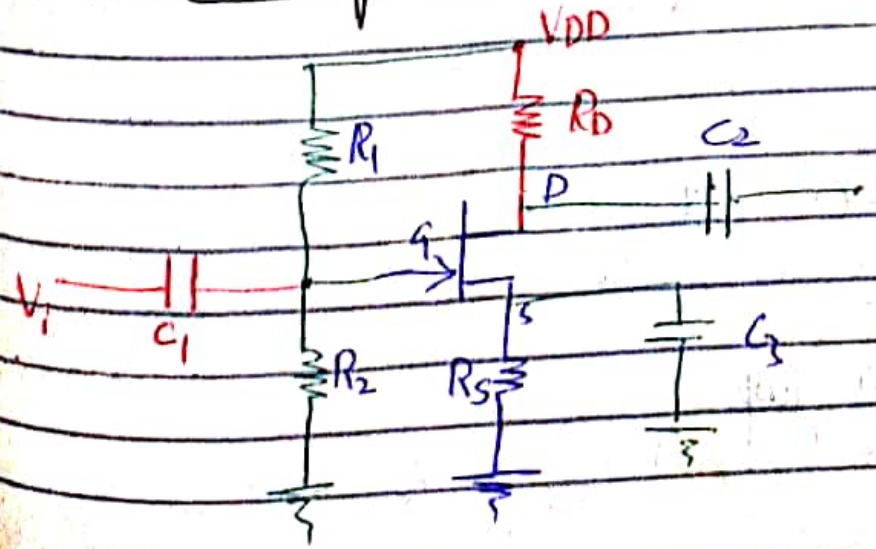
$V_{DS} = V_{DD} - I_D (R_S + R_D)$

$V_D = V_{DD} - I_D R_D$

Q point depends on value of R_S.

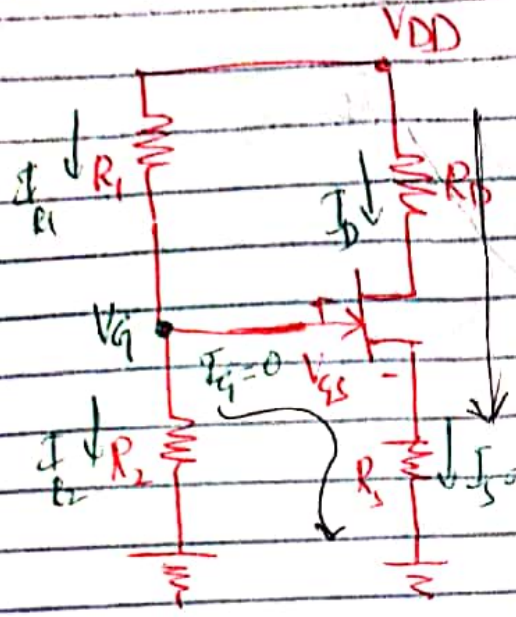
Ex 7-3

Voltage Divider Bias Configuration



common source amplifier with V.D.B n channel JFET.

Open circuit capacitors



KCL

$I_{R1} = I_{R2}$

$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$

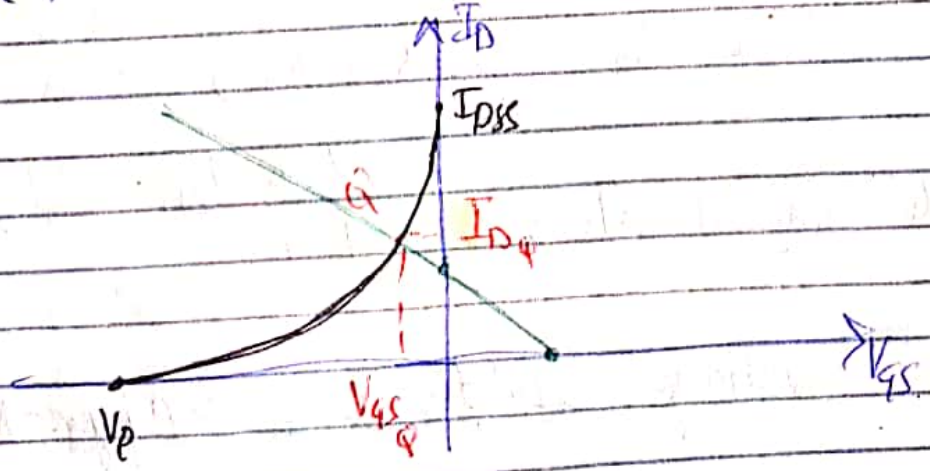
KVL to I/P

$-V_S + V_{GS} + V_{RS} = 0$

$V_{GS} = V_G - V_S$

network eq $\leftarrow$ $\boxed{V_{GS} = V_G - I_D R_S}$

$P_1(0, I_{DSS})$ $P_2(V_P, 0)$ $P_3(V_P/2, I_{DSS}/4)$



first $V_{GS} = 0$ find I_D

next $I_D = 0$ find V_{GS}

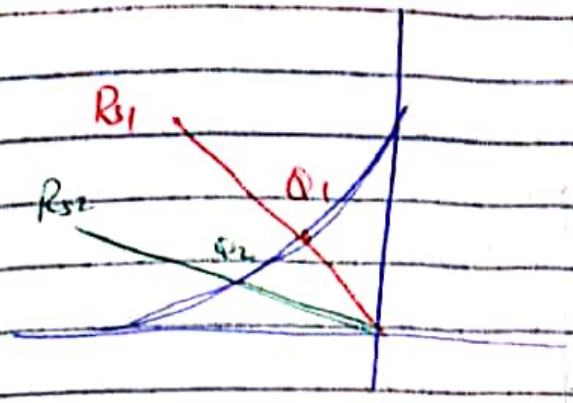
KVL to o/p loop

$-V_{DD} + I_D R_D + V_{DS} + V_{RS} = 0$

$$V_{DS} = V_{DD} - I_D R_D - V_{RS}$$

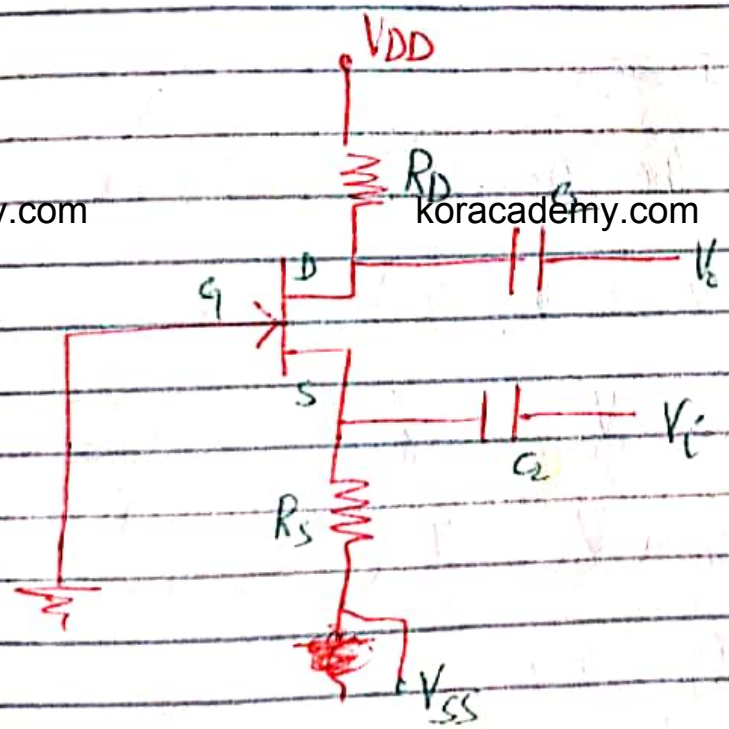
$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Ex 7.5



$R_{S2} > R_{S1}$

Common Gate Configuration:



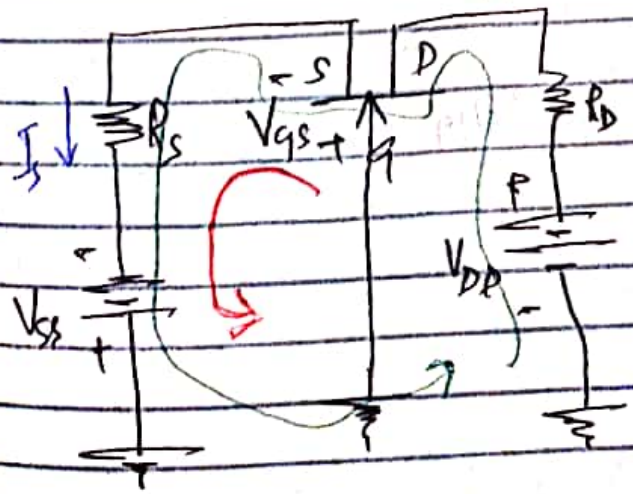
KVL to i/p loop

$$-V_{SS} + V_{GS} + I_S R_S = 0$$

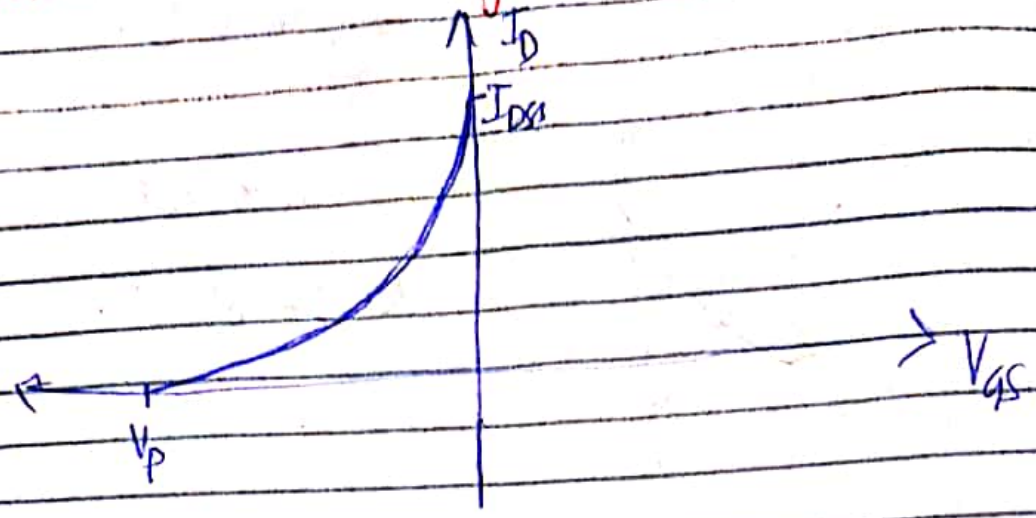
$I_S = I_D$

$$V_{GS} = V_{SS} - I_D R_S$$

Gate mark ✗s.



Transfer Xs are independent of the network in which they are applied.



from load line

$V_{GS} = V_{SS}\big|_{I_D=0}$ $\quad I_D = \frac{V_{SS}}{R_S}\Big|_{V_{GS}=0}$

Apply KVL to the parameters of the circuit

$$-V_{DD} - V_{SS} + V_{DS} + V_{RD} + V_{RS} = 0$$

$$-V_{DD} - V_{SS} + V_{DS} + I_D R_D + I_D R_S$$

$$V_{DS} = V_{DD} + V_{SS} - I_D(R_S + R_D)$$

Similarly $V_D = V_{DD} - I_D R_D$

$V_S = -V_{SS} + I_D R_S$

Lecture 4: 14/10/19

FET Biasing.

(i) Fixed Bias
(ii) Self Bias
(iii) Voltage divider bias

(N) Common gate configuration.

Reverse transfer is the ratio of input to output.
Forward transfer is the ratio of output to input.

hybrid parameters $h_r = \frac{V_i}{V_o}$ $h_f = \frac{I_o}{I_i}$

- n channel → no +ve V_{GS} is allowed.
- p channel → no −ve V_{GS} is allowed.
- JFET operates only in one mode → ie depletion mode.

Voltage divider rule is applied to series impedances with same amount of current flowing
↳ no restriction on the no. of components.
For current divider rule only the impedances must be connected in parallel.

Depletion Type MOSFET:

- JFET → PN junction is present b/w gate and channel
- Silicon dioxide layer is present b/w metal in gate and channel

Transfer chars of both are almost similar upto I_{DSS}.
- the current may exceed beyond I_{DSS}.

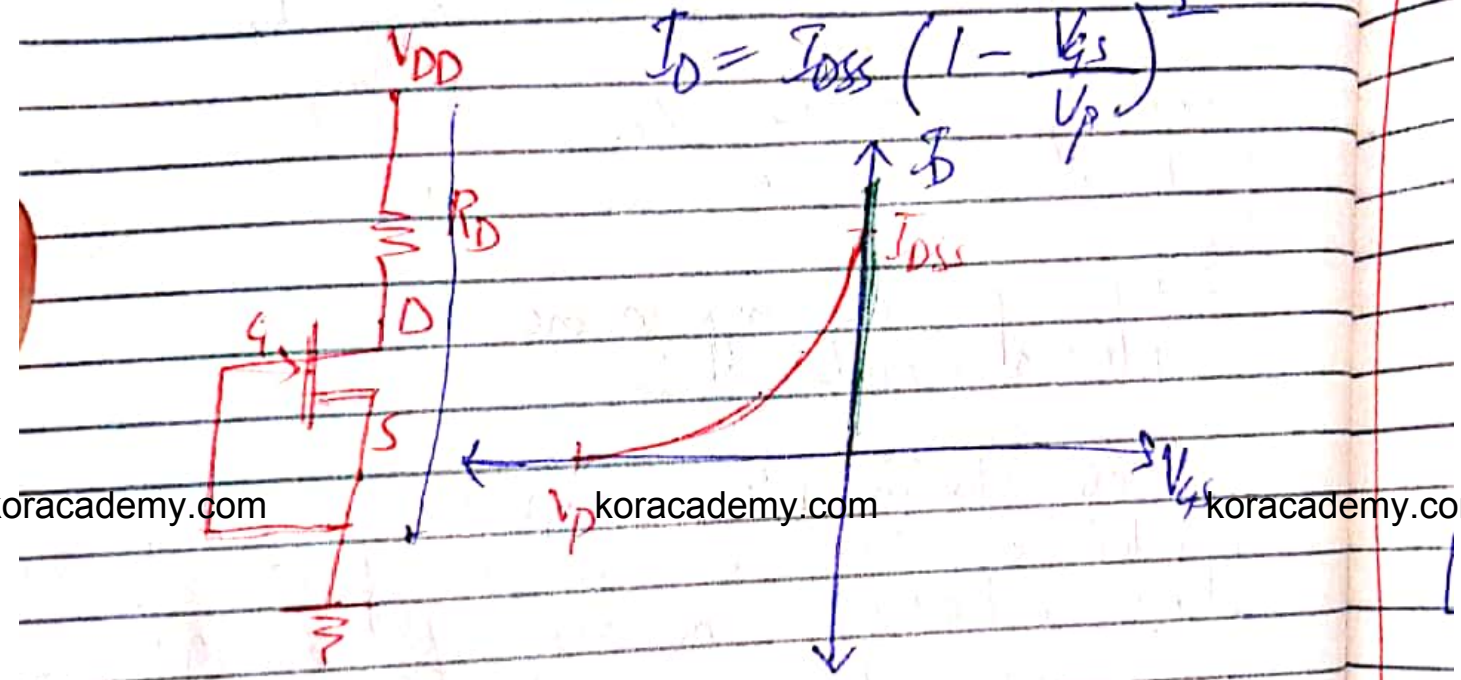
In case of n channel, the transfer curve may enter +ve V_{GS} region → enhancement mode.
- operates in two modes → enhancement
  → depletion.

All the biasing that we have studied yet are also applicable to DMOSFET.

Special Case; $V_{GS} = 0V$

simplest biasing arrangement

n channel JFET.



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

load line $V_{GS} = 0 \Rightarrow I_D = I_{DSS}$, $V_{DS} = 0V$

so Q point $= (0, I_{DSS})$

KVL to the o/p section

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

$V_{DS} = V_D$ as $V_{DS} = V_D - V_S$, $V_S = 0$

$\Rightarrow V_{DS} = V_D$

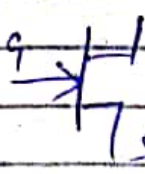
When fourth point determined? When there is Intercept in the load line. $y = mx + c$

DMOSFET:

Shockley Eq is applicable ie $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

4 points are needed to plot transfer Xtns.

n channel JFET



$V_{GS} \leq 0$ V

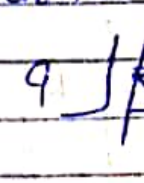
Depletion mode

$V_{GS} = 0$; $I_D = I_{DSS}$ maximum I

$V_{GS} > 0$ not allowed

↳ enhancement mode not allowed

n channel DMOSFET



$V_{GS} < 0$ V

Depletion mode

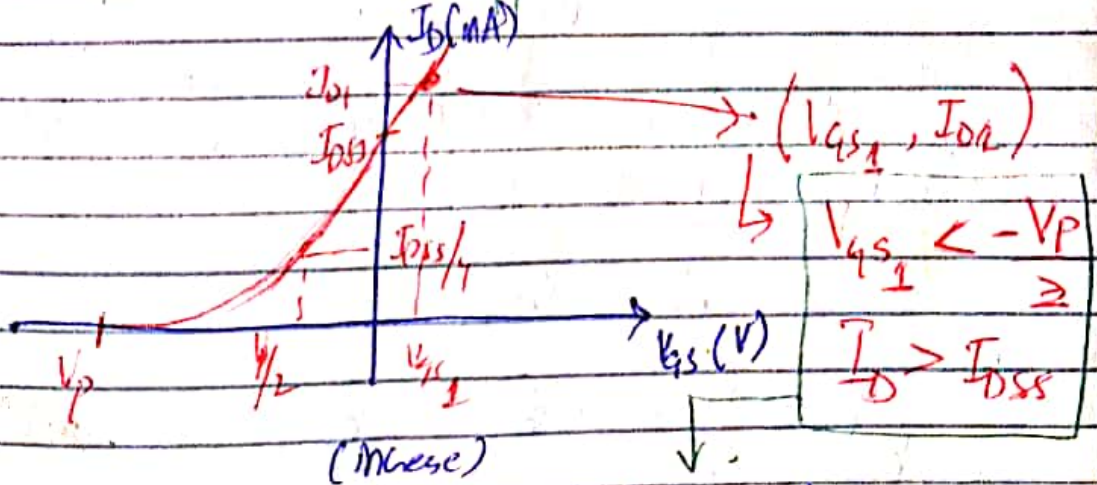
$V_{GS} = 0$ V $I_D = I_{DSS}$ not the maximum I

$V_{GS} > 0$ V allowed

I_D can exceed beyond I_{DSS}

↳ enhancement mode operation.

For p channel the opposite is true.



(increase)

→ small change in V_{GS} will result in very large increase in current I_D. → so to keep it controlled we impose the condition.

n channel → V_P -ve

p channel → V_P +ve

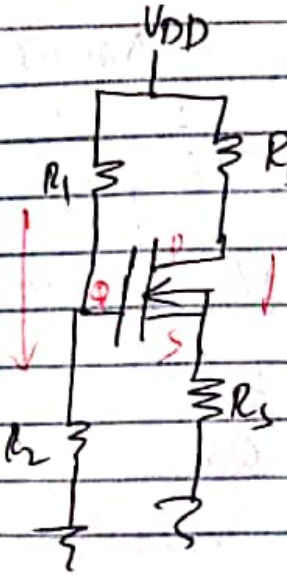
Voltage divider

Ex 2.7 for n DMOSFET, determine $I_{D(Q)}$ and $V_{GS(Q)}$ (a) V_{DS}

$I_{DSS} = 6mA$ $V_P = -3V$

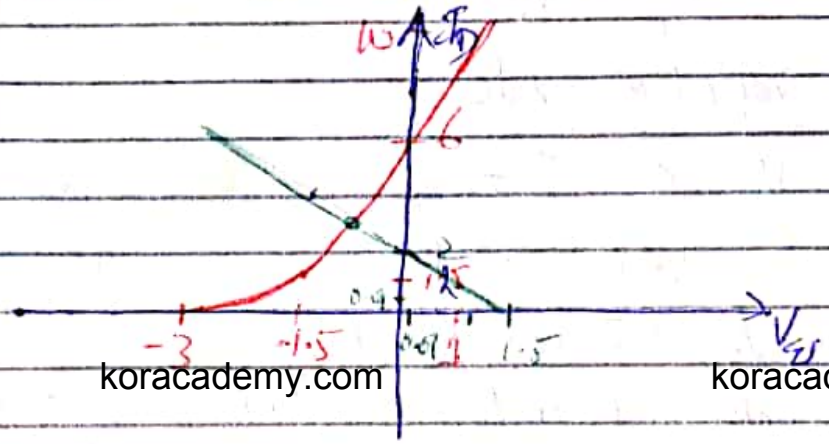
$R_D = 1.8K\Omega$ $V_{DD} = 18V$ $R_1 = 110M\Omega$

$R_2 = 10M\Omega$ $R_S = 750\Omega$



$V_{GS} = V_G - I_D R_S$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$



(1) Device

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$P_1(V_P, 0)$ $P_2(0, I_{DSS})$ $(-1.5, 1.5)$

fourth point? $V_{GS} < 1.5$

$V_{GS} = 1$ $I_D = 6m\left(1 - \frac{1}{-3}\right)^2 = 10^{-6}mA$

(2) Network

$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = 1.5V$

$I_D = \frac{V_G}{R_S} - \frac{V_{GS}}{R_S}$

$$I_D = -\frac{V_{GS}}{R_S} + \frac{V_G}{R_S}$$

$V_{GS} = 0 \Rightarrow I_D = 2mA$ $(0, 2)$

$I_D = 0 \Rightarrow V_{GS} = 1.5V$ $(1.5, 0)$

Q point $(-0.8, 3.1) = (V_{GSQ}, I_{DQ})$ ANS

Now $V_{DS} = 18 - 3.1m(1.8K + 0.7K)$

$= 18 - 3.1 \times 10^{-3}(2.5 \times 10^3)$

$= 18 - 7.75$

$V_{DS} = 10.25$ $(10.1\ V)$ true

Repeat for $R_S = 150\,\Omega$.

The transfer curve will be the same.

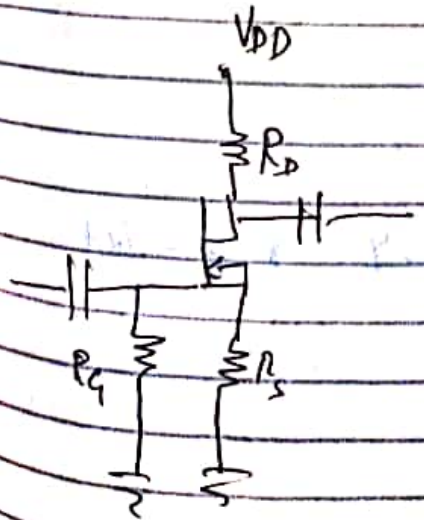
For load line; $I_D = -\left(\frac{1}{R_S}\right)V_{GS} + \frac{V_q}{R_S}$

$V_{GS} = 0 \Rightarrow I_D = 0.01$ $(0, 0.01)$

$I_D = 0 \Rightarrow V_{GS} = 1.5$ $(1.5, 0)$

$R_S \downarrow$ Intercept $\uparrow$

Self Biased Network Q point conducts, V_D,



terminal i/p → terminal o/p with 180° phase shift ∴ ISO.

Common source amplifier provides

↳ In BJT → Common Emitter.

The voltage gain for common source / C.E is negative

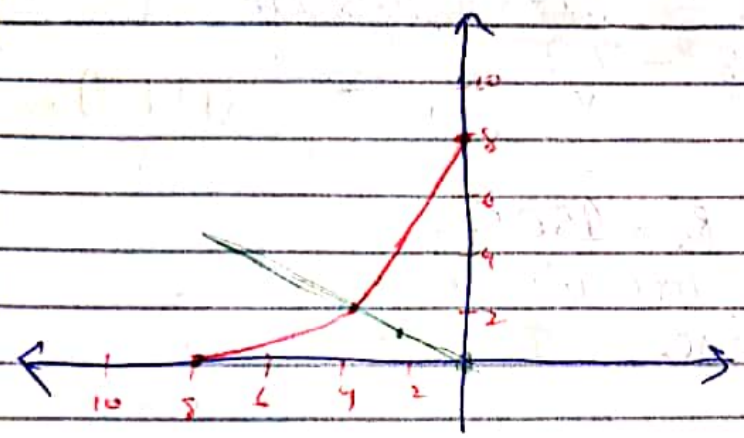
Device chs don't change with the network.

$V_{DD} = 20V \quad R_S = 2.4k\Omega \quad R_G = 1M\Omega$

$V_p = -8 \quad I_{DSS} = 8mA$

$V_{GS} = -I_D R_S \rightarrow$ network

$V_{DS} = V_{DD} - I_D(R_D + R_S)$



$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

$(V_p, 0) = (-8, 0) \quad (0, I_{DSS}) = (0, 8mA)$

$(V_p/2, I_{DSS}/4) = (-4, 2)$

→ load line $I_D = -\frac{V_{GS}}{R_S}$

$I_D = 0 \Rightarrow V_{GS} = 0$

$V_{GS} = 0 \rightarrow I_D = 0$ $\quad V_{GS} = 2.4 \Rightarrow I_D = 1mA$

Special case

$V_{GS} = 0$

$I_{DQ} = I_{DSS}$

Biasing of Enhancement Type MOSFET

- EMOSFET doesn't contain channel physically. Construction wise D and EMOSMET are almost similar.

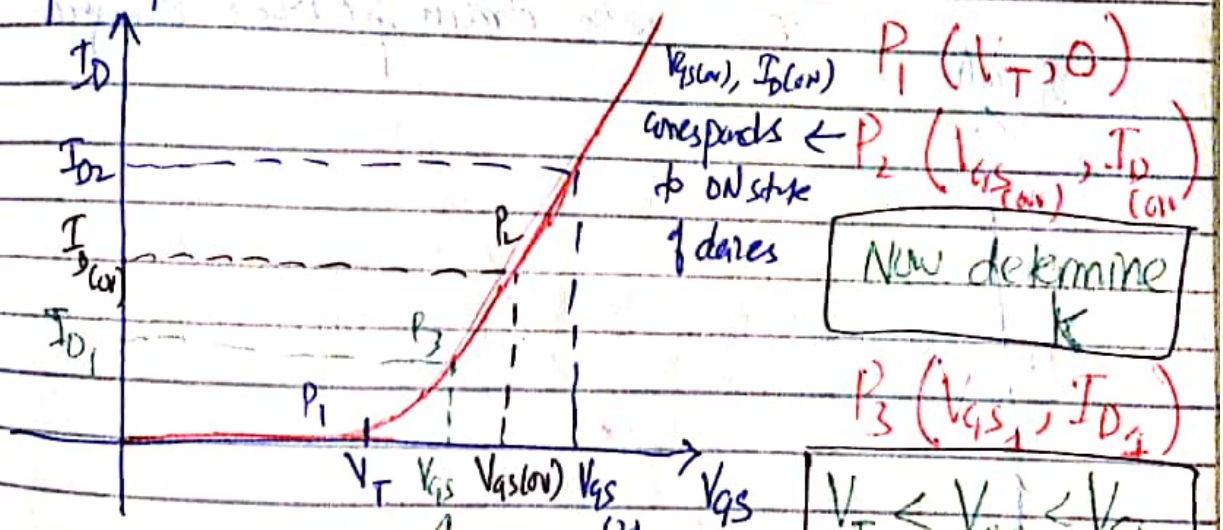
→ Shockley Eq is not applicable but still I_D and V_{GS} are related non linearly.

$$I_D = K(V_{GS} - V_T)^2 \qquad K = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

V_T → threshold voltage

EMOSFET are provided with 3 parameters in data sheet; V_T, $I_{D(on)}$, $V_{GS(on)}$

To draw the transfer curve for EMOSFET, four points are needed.



$P_1(V_T, 0)$

$P_2(V_{GS(on)}, I_{D(on)})$

Now determine K

$P_3(V_{GS_1}, I_{D_1})$

$V_T < V_{GS} < V_{GS(on)}$

$P_4(V_{GS_2}, I_{D_2})$

$V_{GS(2)} > V_{GS(on)}$

$V_{GS} \leq V_T$

$\Rightarrow I_D = 0$ → Why?

B/c there is no channel

$$V_G = \left(\frac{R_2}{R_1+R_2}\right)V_{DD} \quad \text{at } I_G = 0mA$$

$$V_{GS} = V_G - I_D R_S \rightarrow \text{load line}$$

$$I_D = \frac{V_G}{R_S} - \frac{V_{GS}}{R_S} \qquad y = mx + c$$

$$V_{GS} = V_G\Big|_{I_D=0} \qquad I_D = \frac{V_G}{R_S}\Big|_{V_{GS}=0V}$$

Find V_{DS}

KVL to o/p loop $\quad V_{DD} = I_D R_D + V_{DS} + I_D R_S$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Lecture 5 21/10/19

Quiz 1 Perform the dc analysis of n channel DMOSFET common source amplifier with voltage divider biasing using graphical approach

Chapter 8 :

AC Analysis Of FET Amplifiers

DC analysis → to bias the circuit properly → establish Q point.

Once Q point is established (ckt is biased) then apply input AC signal to get an amplified output signal.

If not properly biased → distorted output.

Signal is something that carries information.

FET is a unipolar, high input impedance devi
↳ $10^{12} - 10^{15}\ \Omega$

b/c of presence of SiO_2 layer ← ↳ MOSFET i/p z

i/p current = 0 ← ↳ open circuit equivalent

current gain is undefined. b/w i/p terminals in FET.

↳ (JFET, MOSFET, MESFET).

Small subscript represents AC quantity.

$$\text{Resistance} = \frac{V}{I} \qquad \text{Conductance} = \frac{I}{V}$$

FET ⇒ i/p = V_{gs} o/p = I_d

$$\text{Trans conductance} = \frac{I_d}{V_{gs}}$$

AC analysis ⇒ Small signal equivalent model

AC analysis is performed to determine;

(i) AC voltage gain.
(ii) i/p impedance
(iii) o/p impedance.

} circuit features/parameters.

Two important parameters before developing model

g_m and

g_m → transconductance, → relationship b/w. i/p and o/p quantities

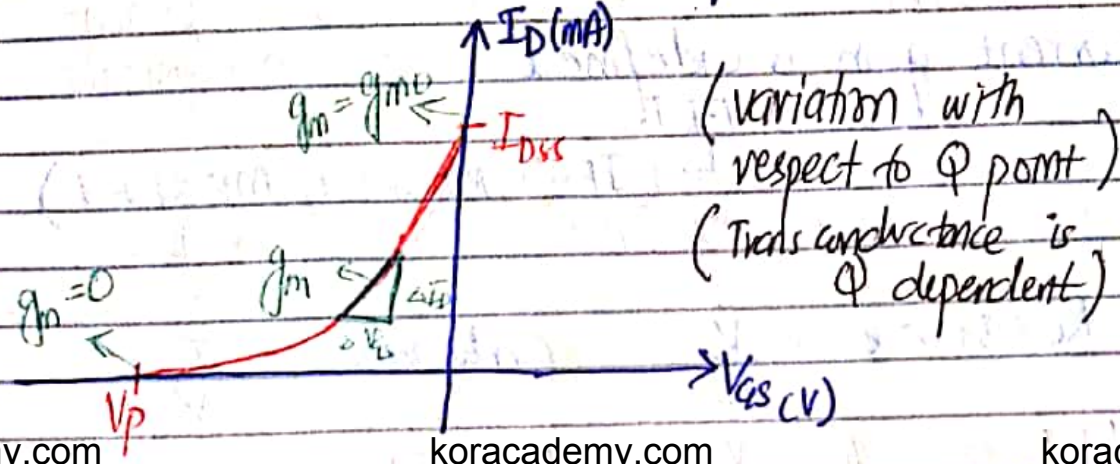
Graphical

$g_m = ?$

Let we start with JFET

① Draw the transfer Xtics of the device with help of shockley's equation. and establish Q point.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



(variation with respect to Q point)
(Trans conductance is Q dependent)

The slope line (tangent line) thro Q point represents Trans conductance.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

unit mho ℧ or semen

As we move up g_m increases.
move down g_m decreases.

Corresponds to $V_{GS} = 0$

As $I_D \to I_{DSS}$, $V_{GS} \to 0 \Rightarrow g_m \to g_{m_0} \to$ 3000

As $V_{GS} \to V_P$, $I_D \to 0$, $g_m \to 0$

The relationship b/w g_m and V_{GS} is reciprocal

Limitation? Accuracy more points → more accuracy

Ex 8.1, 8.2

Mathematical Approach:

"The derivative of a function at a point is equal to the slope of the tangent line drawn at that point."

We have Shockley Eq. Take its derivative wrt V_{GS}.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}}\left[\left(1 - \frac{V_{GS}}{V_P}\right)^2 I_{DSS}\right]$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$g_m = 0 \,|_{V_{GS}=V_P}$ $\quad g_m = \frac{2I_{DSS}}{|V_P|}\,|_{V_{GS}=0}$

$\hookrightarrow g_{m0} = \frac{2I_{DSS}}{|V_P|}$

$$\Rightarrow g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

Plot s/w g_m and V_{GS}.

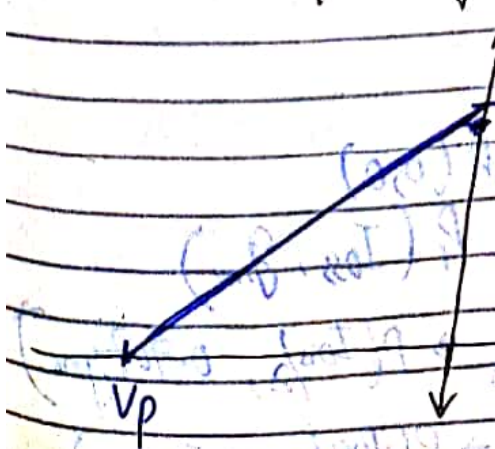
linear → two points

$g_m = g_{m0} \,|_{V_{GS}=0}$

$g_m = 0 \,|_{V_{GS}=V_P}$

$P_1 \Rightarrow (V_P, 0)$

$P_2 \rightarrow (0, g_{m0})$



In the specification sheet g_m is given as Y_{fs}.

$y \rightarrow$ admittance

$f \rightarrow$ forward transfer parameter.
↳ o/p ÷ i/p

reverse i/p ÷ o/p

$S \rightarrow$ connected to source terminals.

For JFET 1000 - 5000 μ siemens or 1 msiem - 5 m

Effect of I_D on g_m?

Rearranging the shockley's equation;

$$\left(1 - \frac{V_{GS}}{V_P}\right)^2 = \frac{I_D}{I_{DSS}}$$

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

As $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$

$$g_m = g_{mo}\sqrt{\frac{I_D}{I_{DSS}}}$$

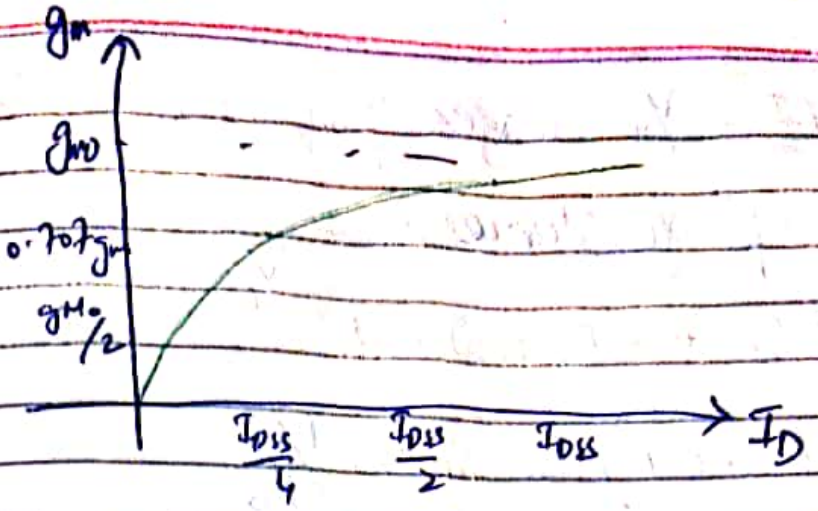
Plot of g_m vs I_D.

$I_D = 0 \Rightarrow g_m = 0 \Rightarrow P(0,0)$

$I_D = I_{DSS} \Rightarrow g_m = g_{mo} \Rightarrow P_1(I_{DSS}, g_{mo})$

$I_D = I_{DSS}/2 \Rightarrow g_m = 0.707\, g_{mo} \Rightarrow P(I_{DSS}/2, 0.707\, g_{mo})$

$I_D = I_{DSS}/4 \Rightarrow g_m = g_{mo}/2 \Rightarrow P(I_{DSS}/4, 0.5\, g_{mo})$



g_{mo} → Value of g_m when $V_{GS} = 0V$

JFET Input Impedence (Z_i)

Z_i is sufficiently large such that input terminals approximate an open circuit equivalent.

$$Z_i \text{ (JFET)} \cong \infty$$

JFET A practical value of $10^9 \Omega$ is typical.

For MOSFET and ~~CMOSFET~~ a ~~typical value~~ 10^{12} to 10^{15} is typical.

On the minimum side, the Impedance of MOSFET is 1000 times more than JFET.

$$\left(\frac{10^{12}}{10^9} = 1000\right).$$

JFET Output Impedance (Z_o)

Same as BJT.

Available in the specification sheet as Y_{os} ↵

is the component of admittance eq circuit

o → o/p network parameter

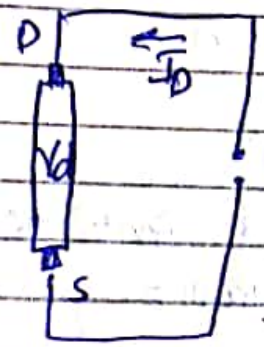
s → source terminal to which it is attached in the model.

For JFET, Y_{os} ranges from 10 μS to 50 μS

In terms of resistance $Z_o = \frac{1}{Y_{os}}$

20 KΩ ↔ 100 KΩ

Z_o (JFET) = $r_d = 1/Y_{os}$



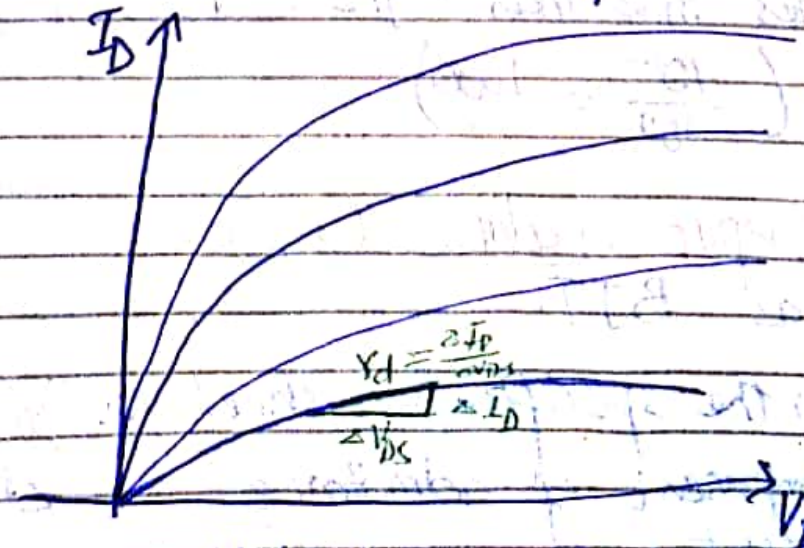
$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ | V_{GS} = constant

↳ Require drain X-hrs.

→ Tangent line on Q point give r_d.

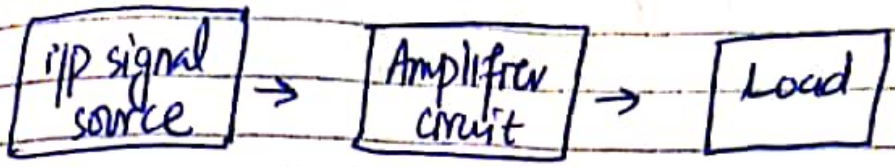
More horizontal the line, less will be the slope. → more will be the resistence.

For ideally horizontal line (slope = 0), the resistance will be infinite



The model should reflect the voltage controlling property of JFET.

Transducer → converts one form of energy to another
eg microphone converts mechanical to electrical.



For the i/p signal source amplifier acts as a load and for the load it acts a source.

→ The drain current I_D depends on two quantities : V_{DS} and V_{GS}.

$$I_d = V_{gs} g_m + \frac{V_{ds}}{r_d}$$

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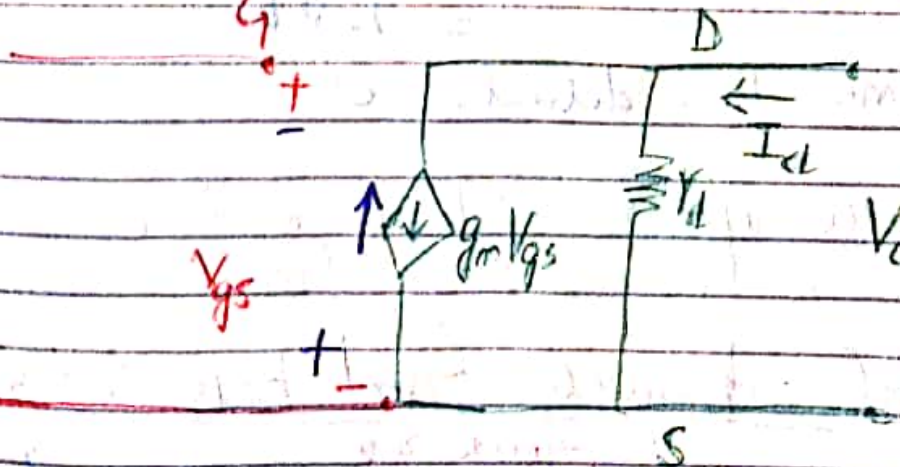
$$g_m = \frac{\partial I_d}{\partial V_{gs}}\Big|_{V_{ds}=\text{constt}} \qquad r_d = \frac{\partial V_{ds}}{\partial I_d}\Big|_{V_{GS}=\text{constt}}$$

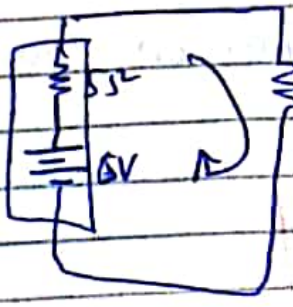
r_d → channel resistance $g_m V_{gs}$ → voltage controlled current source.



If we change the polarity of V_{GS} → direction of current source changes.
i/p terminal open circuit → $I_G = 0$ → reverse biased.

① C.D ⇔ Common collector → emitter follower
Common drain is also called source follower.
$A_V < 1$
Application of emitter follower ⇒ (i) Buffer
(ii) Impedance matching

② Common source ⇔ Common emitter
③ Common Gate ⇔ Common Base



$I = \frac{6}{5+1} = 1A$

$\hookrightarrow P = I^2 R_L = 1 \times 1 = 1W$

So very less power is transfered to load.

If $R_L = 5\Omega$

$I = \frac{6}{5+5} = 0.6A$

$P_L = I^2 R_L = (0.6 \times 0.6)\, 5$

$= 1.8W$

max Power delivered.

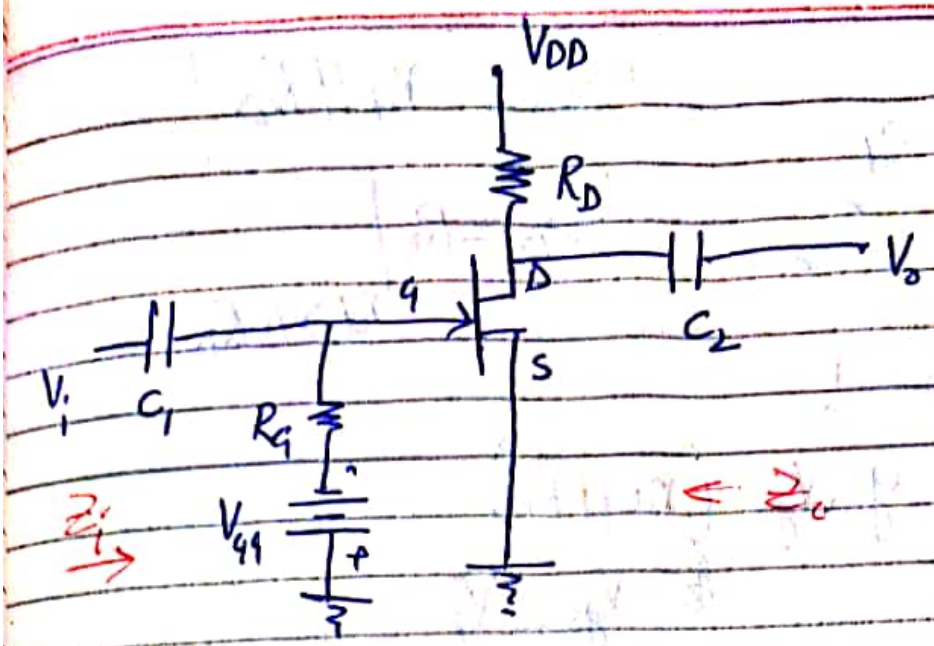
Source impedance = load impedance ⇒ Maximum power is transfered from source to load.

AC Analysis of Fixed Bias Configuration

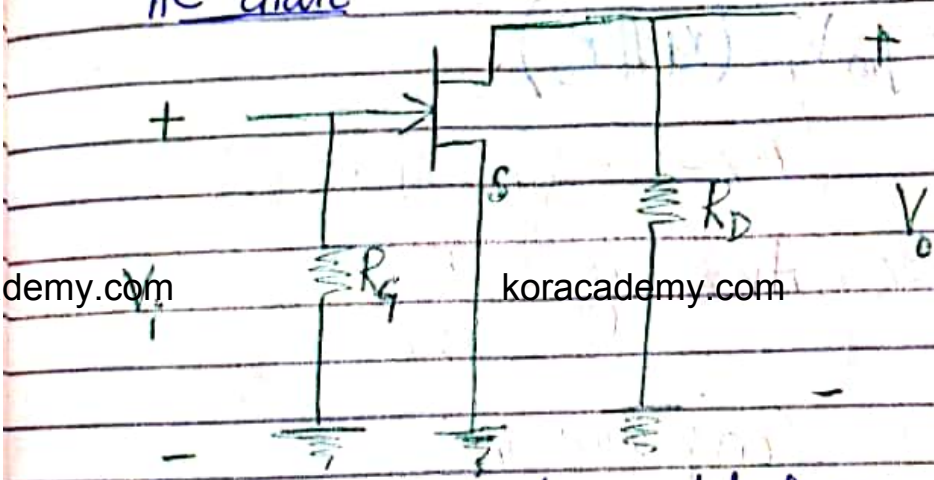
→ made zero

DC sources are grounded and capacitors are replaced by their short circuit equivalents.

Independent V source → Short ckt I source → open ckt

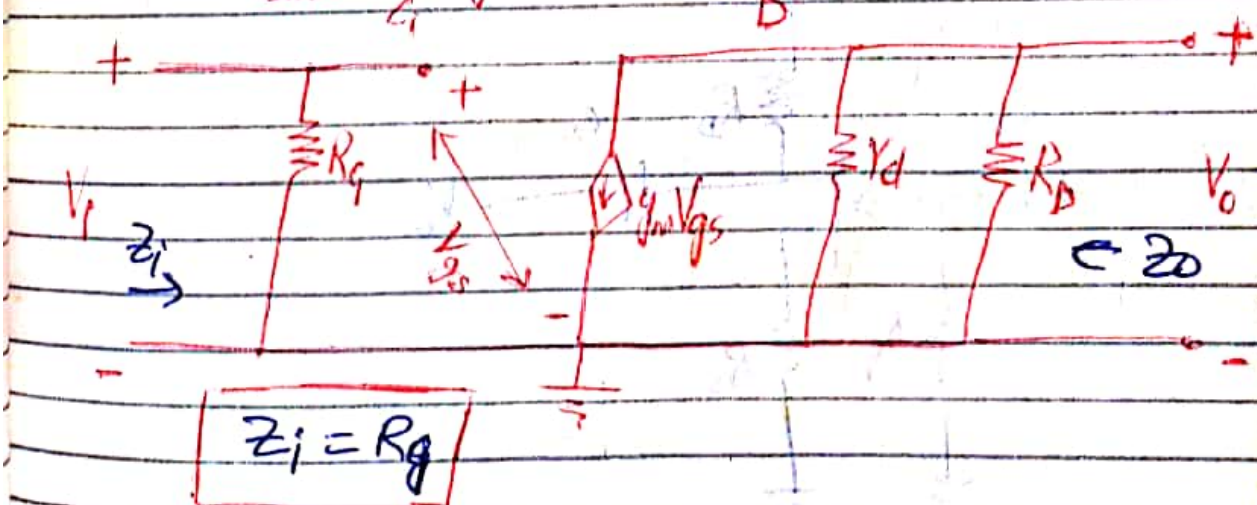


AC circuit



The AC equivalent model is as;

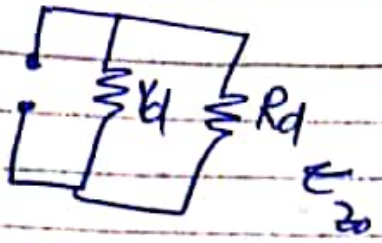
Small signal AC equivalent circuit



$$Z_i = R_g$$

For Z_o, $V_i = 0$ $V_{gs} = 0$

$g_m V_{gs} = 0$



$$Z_o = r_d \,||\, R_D$$

$$Z_o \simeq R_D \Big|_{r_d \geq 10R_D}$$

Voltage gain = ?

$$V_o = -g_m V_{gs} (r_d \,||\, R_D)$$

As $V_{gs} = V_i$

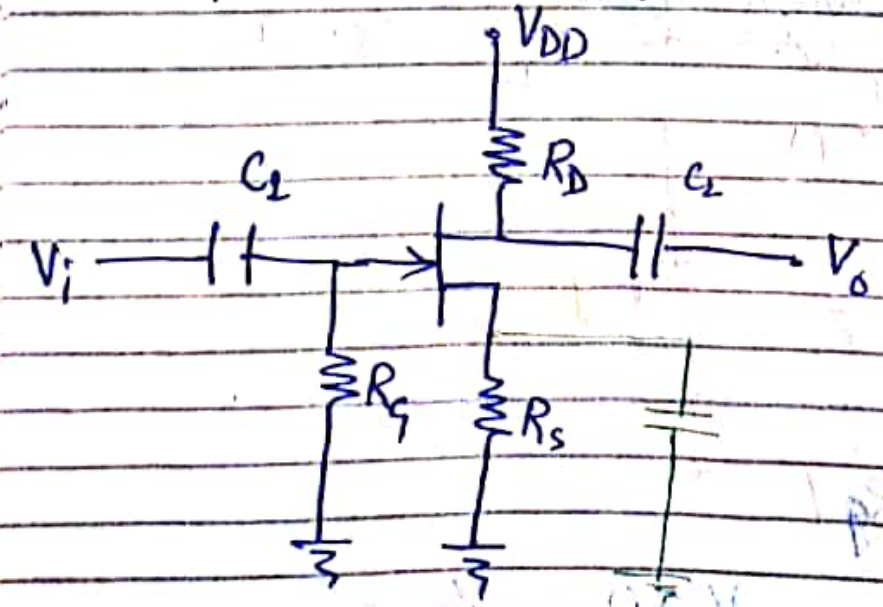
$$V_o = -g_m V_i (r_d \,||\, R_D)$$

$$A_V = \frac{V_o}{V_i}$$

$$A_V = -g_m (r_d \,||\, R_D)$$

or $A_V = -g_m R_D \Big|_{r_d \geq 10R_D}$

Self Bias Configuration



① With bypass capacitor
② Without bypass capacitor

Lecture 6

28/10/19

Q point is also called DC biasing point.

Why AC and DC analysis are performed separately?
Because the circuit property is linear
→ superposition Theorem
→ two sources together → one source at a time
→ then add them together.

The operation of the device is linear w.r.t the Q point.

Amplification → linear operation.
↳ input = sine output = sine
↳ i/p = sine + side o/p = cos sine + side
(sin + cos)

$\sin(A \pm B) = \sin A \cos B \pm \cos A \sin B$
$\cos(A \pm B) = \cos A \cos B \mp \sin A \sin B$

Phase gives starting point to the waveform.
AC analysis → Determine voltage gain, Z_i, Z_o

$Z_i = \infty$ → in JFET b/c PN junction is reverse biased.

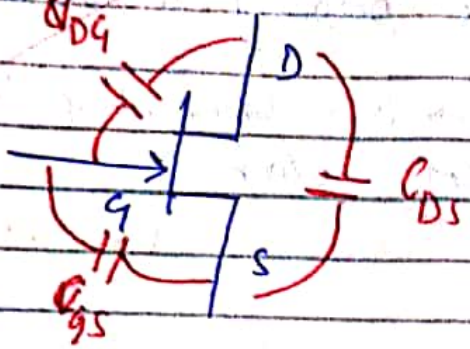
r_d → drain resistance Drain conductance $g_d = \frac{1}{r_d}$
↳ Y_{os} in specification sheet.

AC → requires model → I_d, g_m, V_{gs}, V_{ds}, r_d

Steps for AC analysis.
① Sources removable
② Capacitors short circuit
③ DC equivalent cut
④ Insert AC model for the given transistor.
⑤ Determine A_v, Z_i, Z_o.

Why low freqency AC signal?

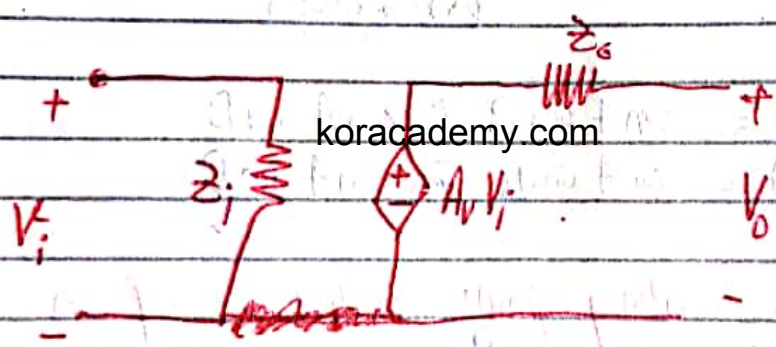
B/c of capacitors. $X_C = \frac{1}{2\pi f C}$



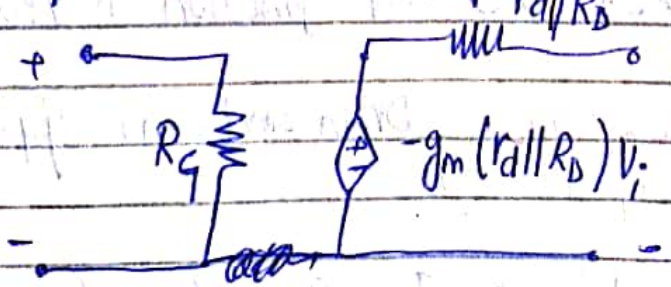
$f \uparrow \quad X_C \downarrow$

port → pair of terminals.

Once we determine A_v, Z_i, Z_o we can draw a two port model.



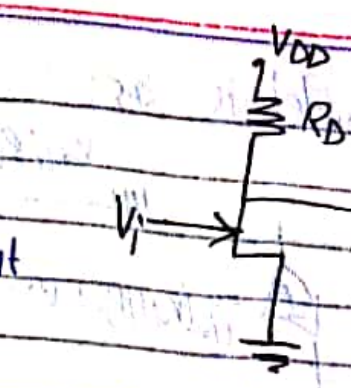
For fixed bias configuration.



As $Z_i = R_G \quad Z_o = r_d \| R_D \quad A_v V_i = -g_m(r_d \| R_D) V_i$

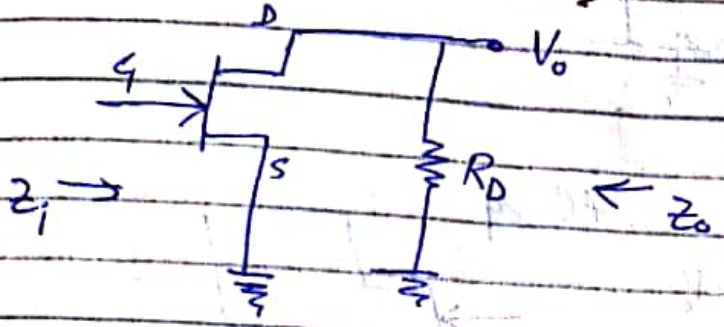
For n channel JFET Common Source Amplifi Voltage Divider

Consider

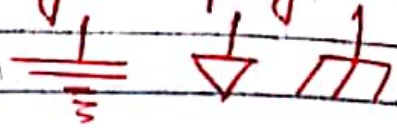


This R_D acts as a resistive load.

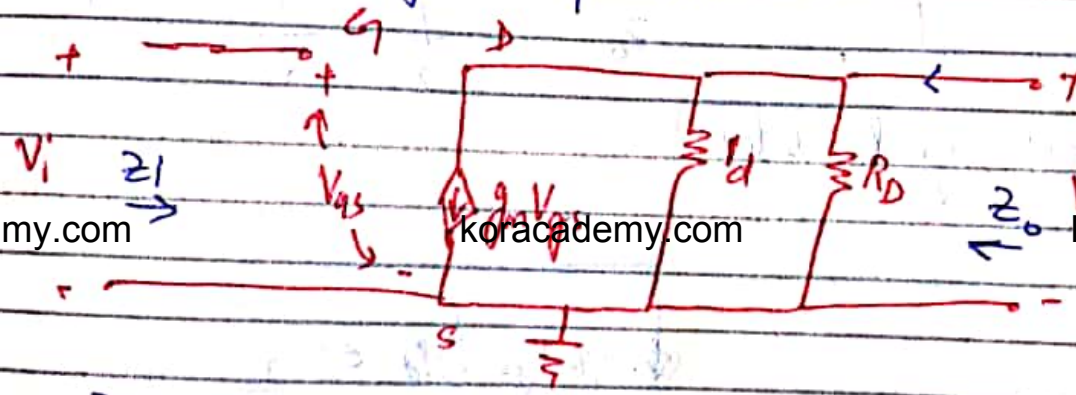
AC equivalent



Symbols for ground.

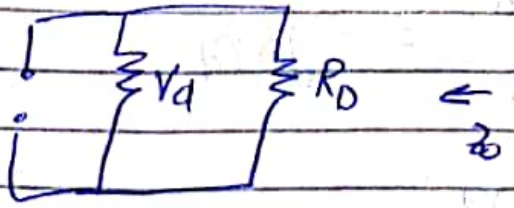


The small signal equivalent model.



$Z_i = \infty$ $Z_o = ?$

For $Z_o \Rightarrow V_i = 0 \Rightarrow V_{gs} = V_i = 0 \Rightarrow g_m V_{gs} = 0$

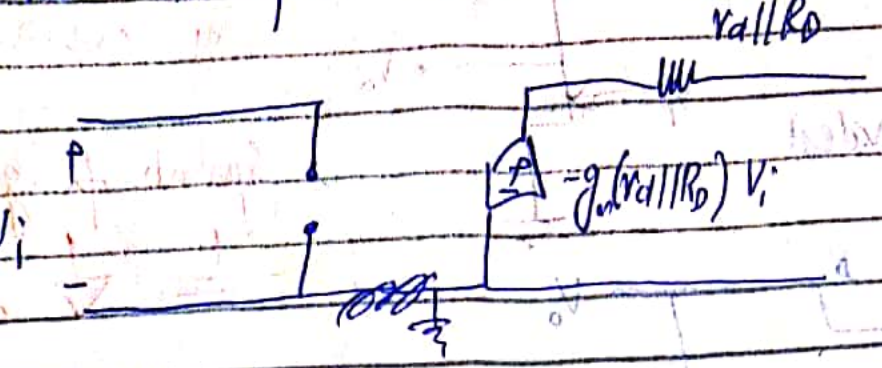


$Z_o = r_d \| R_D$

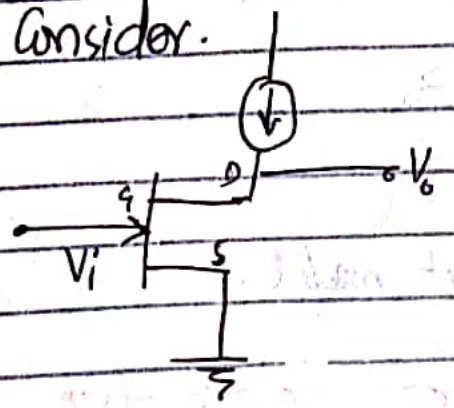
$$V_o = -g_m V_{gs} (r_d \| R_D) = -g_m V_i (r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

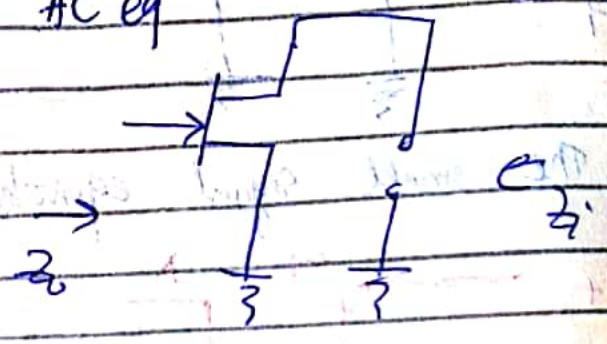
The two port model is as;



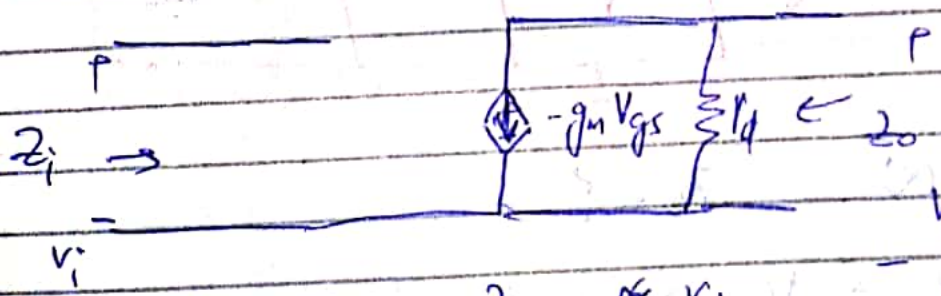
Consider.



AC eq



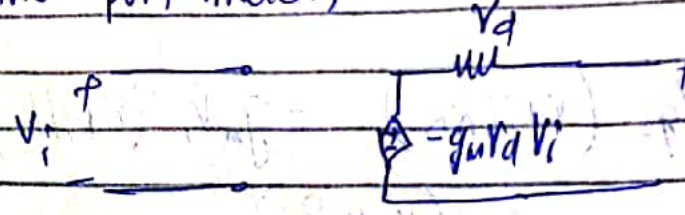
Small signal model



$Z_i = \infty \qquad Z_o = r_d$

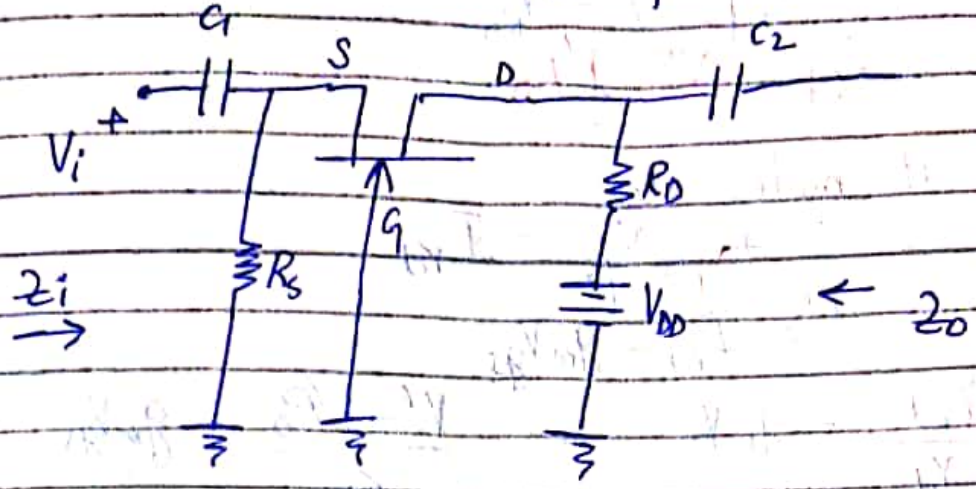
$$A_v = \frac{V_o}{V_i} = \frac{-g_m r_d V_i}{V_i} = -g_m r_d$$

Two port model;

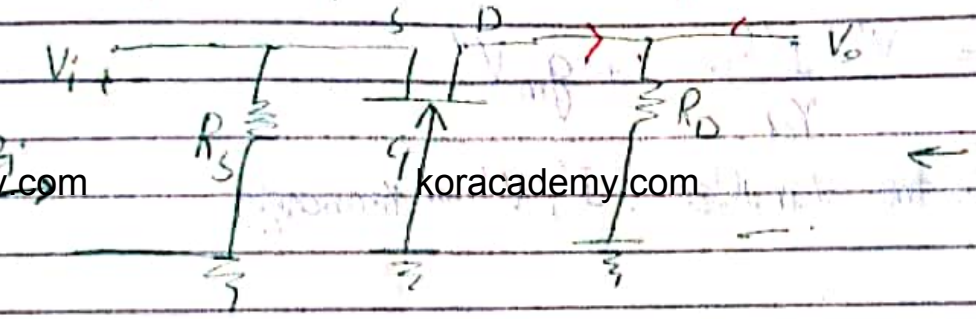


Common Gate Configuration:

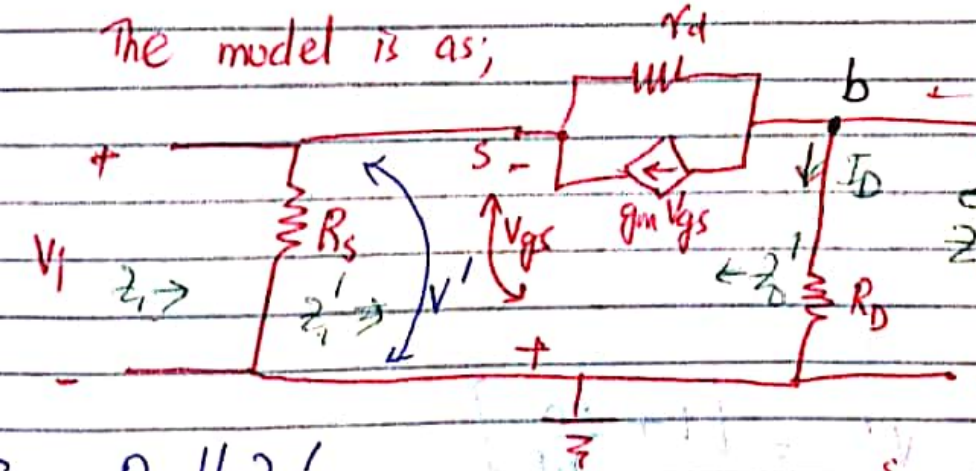
I/P at source O/P from drain



The AC equivalent circuit is as;



The model is as;



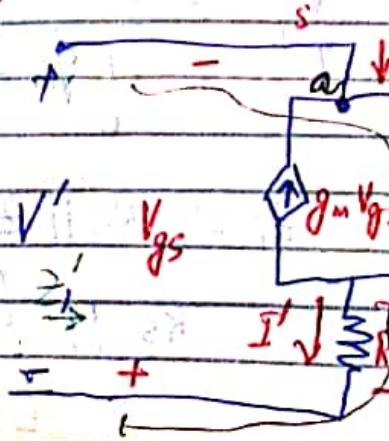
$Z_i = R_S \parallel Z_i'$

Redraw

$Z_i' = \frac{V'}{I'}$

$I' \rightarrow$ unknown

KVL $-V' + V_{rd} + V_{RD} = 0$



$$V' - V_{rd} - V_{RD} = 0$$

$$V_{rd} = V' - V_{R_D}$$

$$V_{rd} = V' - I' R_D$$

KCL at node a.

$$I' + g_m V_{gs} = I_{rd}$$

$$I' = I_{rd} - g_m V_{gs}$$

$$I' = \frac{V_{rd}}{r_d} - g_m V_{gs} = \frac{V' - I' R_D}{r_d} - g_m V_{gs}$$

As $V_{gs} = -V'$ or $V' = -V_{gs}$

$$\Rightarrow I' = \frac{V' - I' R_D}{r_d} + g_m V'$$

↳ two variables I', V' → reamange

Now $$Z_i' = \frac{V'}{I'} = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]}$$

Now $$Z_i = R_S \| Z_i'$$

$$Z_i = R_S \| \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]}$$

Approximating $r_d \geq 10 R_D$ $\quad g_m >> \frac{1}{r_d}$

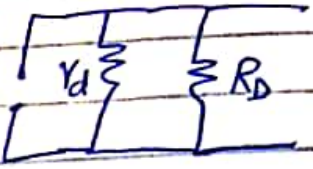
$\Rightarrow Z_i \simeq R_s \,||\, \frac{1}{g_m}$

for Z_o.

Making $V_i = 0 \rightarrow R_s$ short cmt

Gate and Sure connected together. $g_m V_{gs} = 0$

Current source = open circuit.



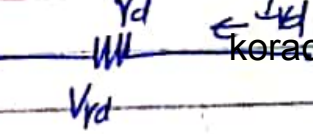
$Z_o = r_d \,||\, R_D$

Voltage gain = ?

$V_i = -V_{gs}$ $\quad V_o = I_D R_D$

$V_{rd} = V_o - V_i \Rightarrow I_{rd} r_d = V_o - V_i$

$I_{rd} = \frac{V_o - V_i}{r_d}$



KCL at node B

$I_{rd} + I_D + g_m V_{gs} = 0$

$I_D = -I_{rd} - g_m V_{gs}$

$I_D = \frac{V_i - V_o}{r_d} + g_m V_{gs}$

Put value of I_D in $V_o = I_D R_D$

Separate V_o and V_i $\rightarrow$ take the ratio.

$A_V = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d} \right]}{\left[1 + \frac{R_D}{r_d} \right]}$

Approximating $r_d \geq 10 R_D$

$\Rightarrow A_V \simeq g_m R_D$

Gain is +ve, so no phase shift.

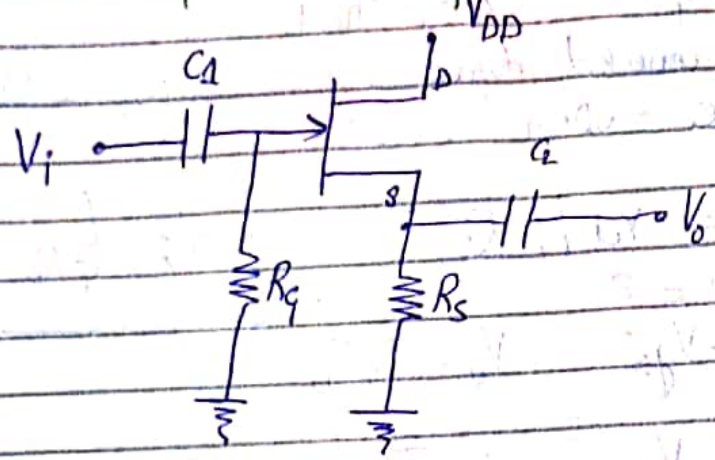
example

Common Drain Amplifier (Source follower)

Voltage gain is less than 1.

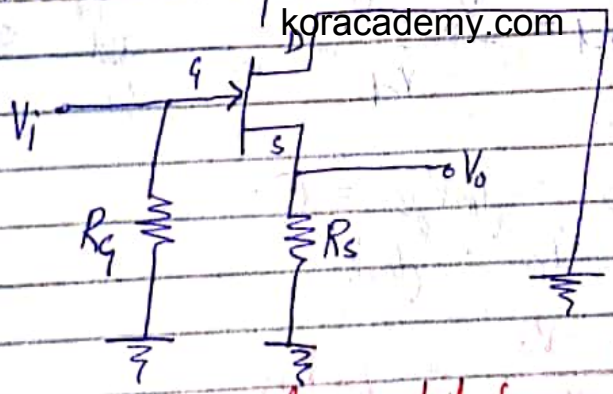
i/p at gate o/p from source.

No phase shift.

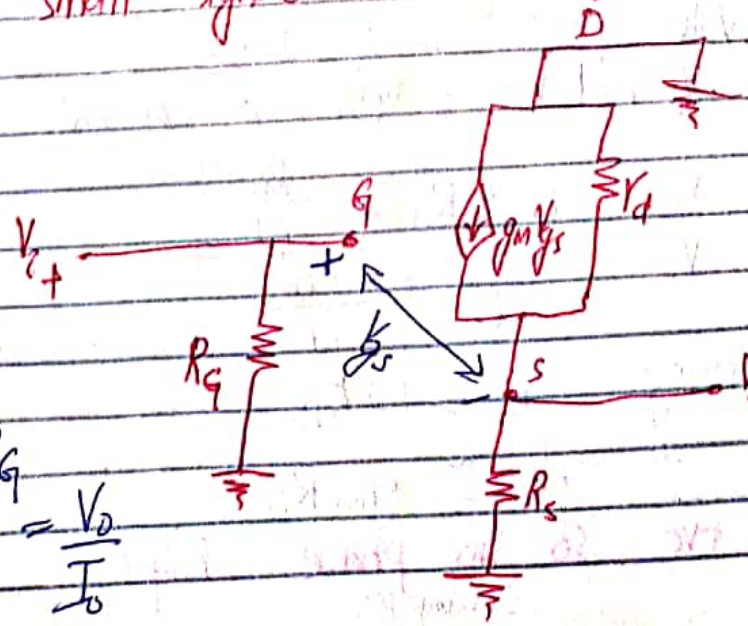


How is gate common?
When signal is applied drain is connected to ground.

The AC equivalent model is as;



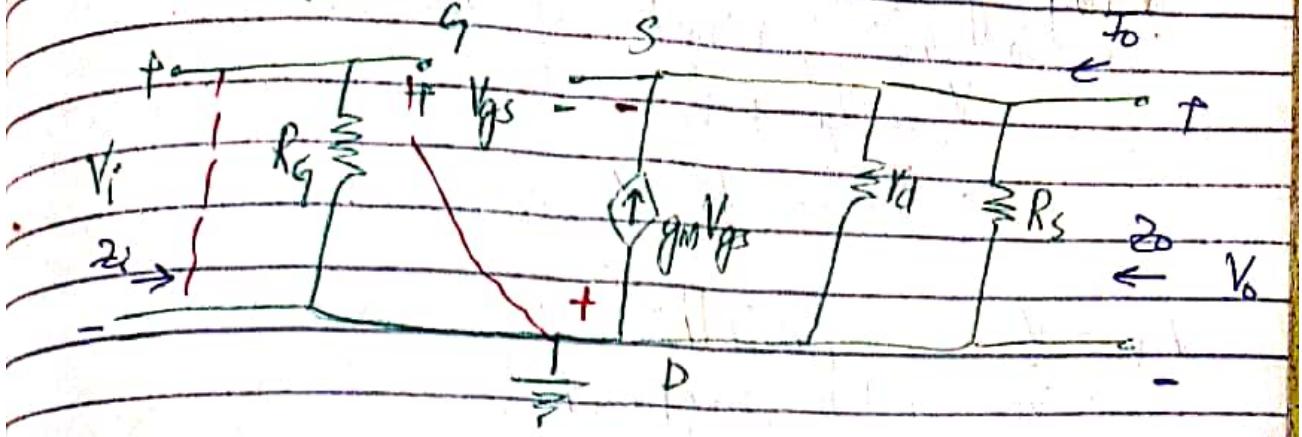
The small signal model is as;



$Z_i = R_G$

$Z_o = \frac{V_o}{I_o}$

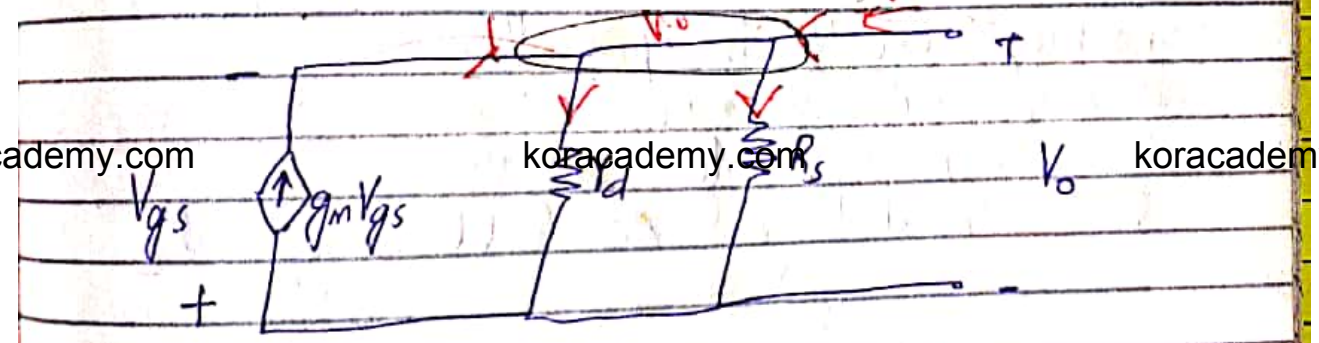
Rearranging



When $V_i = 0$ Gate is connected to ground.

$\hookrightarrow V_o = -V_{gs}$

$V_o = V_{sg} = -V_{gs} \Rightarrow V_{sg} = -V_{gs}$



$I_o + g_m V_{gs} = I_{r_d} + I_{R_s}$

$I_o - g_m V_o = \frac{V_o}{R_s} + \frac{V_o}{r_d}$

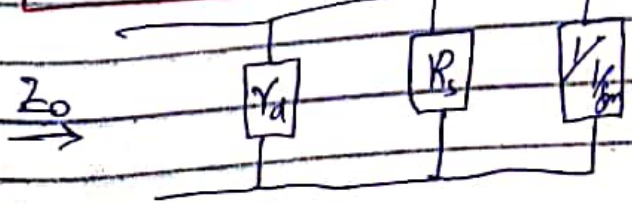
Impedences and resistances are added in series.

$I_o = V_o\left(\frac{1}{R_s} + \frac{1}{r_d} + g_m\right)$

$Z_o = \frac{V_o}{I_o} = \frac{1}{1/r_d + 1/R_s + g_m}$

Conductances are added in parallel

$\Rightarrow \boxed{Z_o = \frac{1}{1/r_d + 1/R_s + 1/(1/g_m)}}$



$V_o = g_m V_{gs} (r_d // R_D)$

Voltage gain?
KVL to the parameter of the circuit.

$V_i = V_{gs} + V_o$

$\Rightarrow V_{gs} = V_i - V_o$

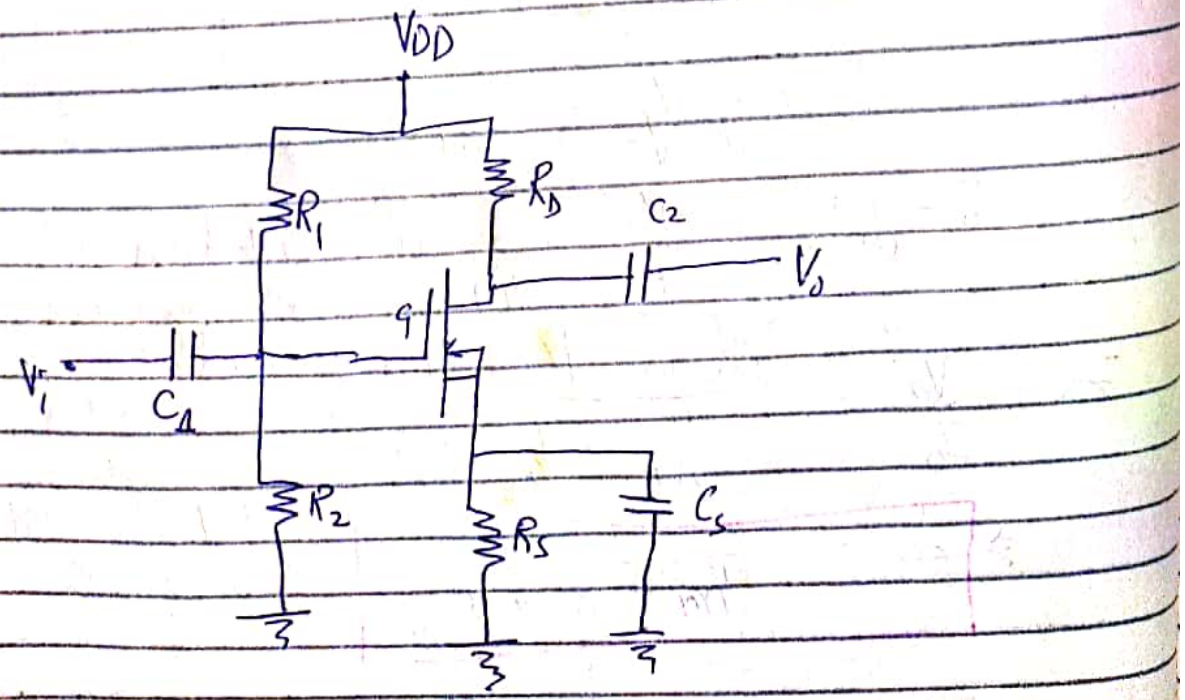
$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d // R_s)}{1 + g_m(r_d // R_s)}$$

$A_v < 1$

$A_v = +ve \rightarrow$ I/P and O/P are in phase.

Depletion Type MOSFET

→ Shockley equation is applicable.
→ Same steps for DC analysis.
→ Same steps for AC analysis.
→ Same small signal AC model is applicable.



$Z_i = R_1 \| R_2 \qquad Z_o = r_d \| R_D$

$A_v =$

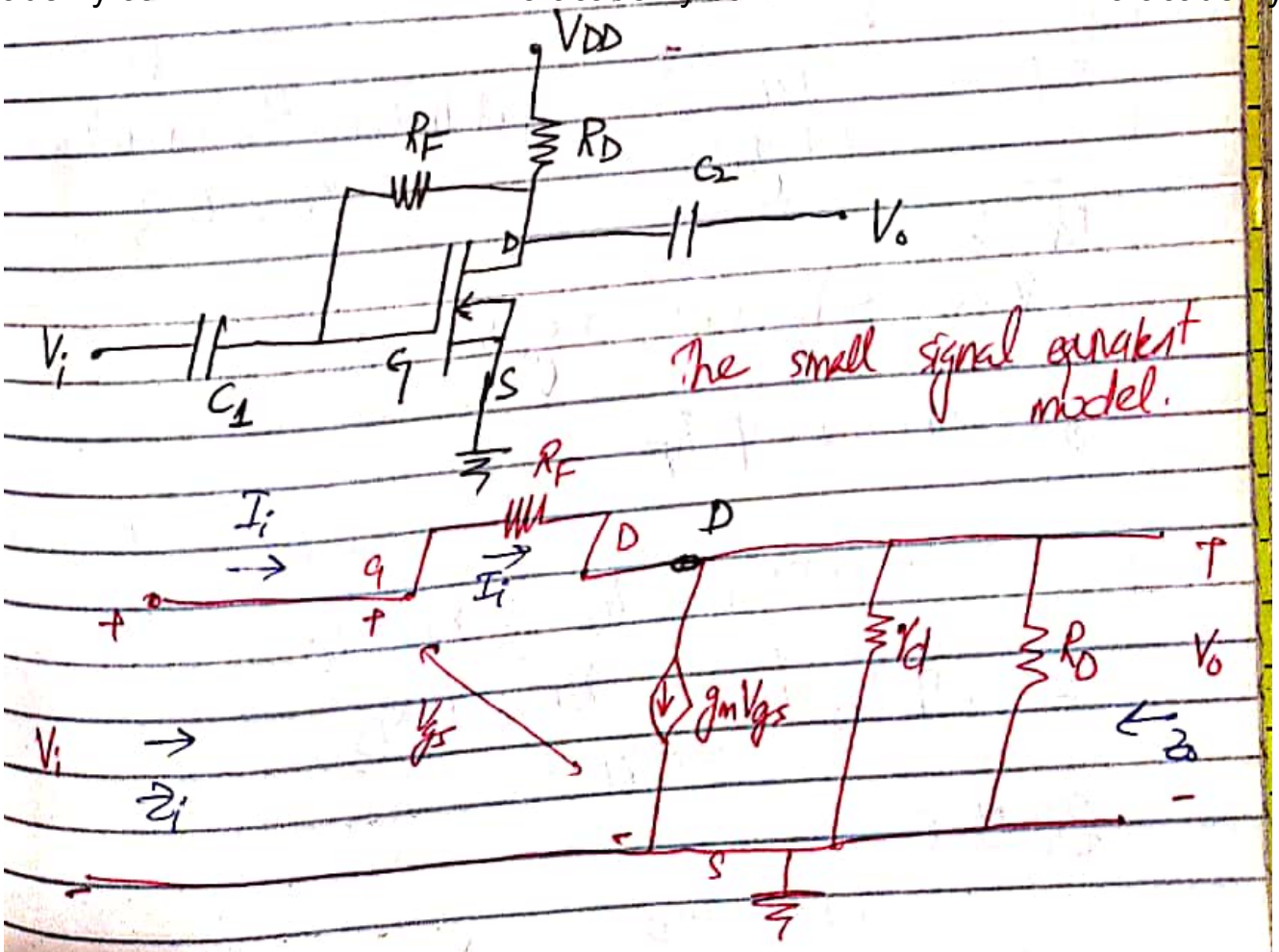
Enhancement type MOSFET → drain feedback, → voltage divider

→ The same model is applicable.
→ Shockley equation is not applicable.
→ $I_D = K(V_{GS} - V_T)^2$ is applicable

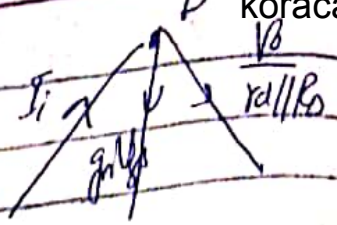
Take derivative wrt V_{GS}

$$g_m = \frac{dI_D}{dV_{GS}} = 2K(V_{GS} - V_T)$$

EMOSFET Drain feedback configuration:



$$Z_i = \frac{V_o}{I_i}$$



Apply KCL at node D.

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

At $V_i = V_{gs}$

$$\Rightarrow I_i = g_m V_i + \frac{V_o}{r_d \| R_D}$$

$$V_o = (I_i - g_m V_i)(r_d \| R_D)$$

And $$I_i = \frac{V_i - V_o}{R_F}$$

$$\boxed{Z_i = \frac{R_F}{1 + g_m R_D}}$$

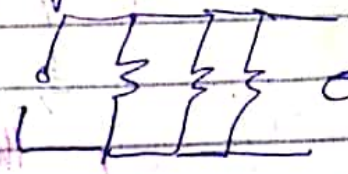
approximated $R_F >> r_d \| R_D$

$r_d \geq 10 R_D$

For Z_o

$V_i = 0 \Rightarrow V_{gs} = 0 \Rightarrow g_m V_{gs} = 0$

$$Z_o = r_d \| R_D \| R_F$$



Approximating ~~$R_F >> r_d \| R_D$~~

~~$r_d \geq 10 R_D$~~

$$Z_o \simeq r_d \| R_D \quad | \; R_F >> r_d \| R_D$$

$$Z_o \simeq R_D \quad | \; r_d \geq 10 R_D$$

$Z_o \cong R_D$ / $R_F \gg r_d \| R_D$, $r_d \geq 10 R_D$

Voltage gain?

Apply KCL to node D.

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

$V_{gs} = V_i$

$$\Rightarrow I_i = g_m V_i + \frac{V_o}{r_d \| R_D}$$

$$\Rightarrow \frac{V_i - V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

Rearrange $\Rightarrow$ V_o on one side, V_i on other side $\rightarrow$ take the ratio

$$A_V = \frac{V_o}{V_i} = \frac{\frac{1}{R_F} - g_m}{\frac{1}{r_d \| R_D} + \frac{1}{R_F}}$$

$$\frac{1}{r_d \| R_D} + \frac{1}{R_F} = \frac{1}{r_d \| R_D \| R_F}$$

Approximating $g_m \gg \frac{1}{R_F}$.

$$A_V \cong \frac{-g_m}{1/r_d \| R_D \| R_F}$$

$1 \div \frac{1}{x} = x$

$$\Rightarrow A_V = -g_m (r_d \| R_D \| R_F)$$

$A_v = -g_m R_D$

Lecture 7 4/11/19

Sidra Smith's Microelectronics

Active load And Passive/Resistive load

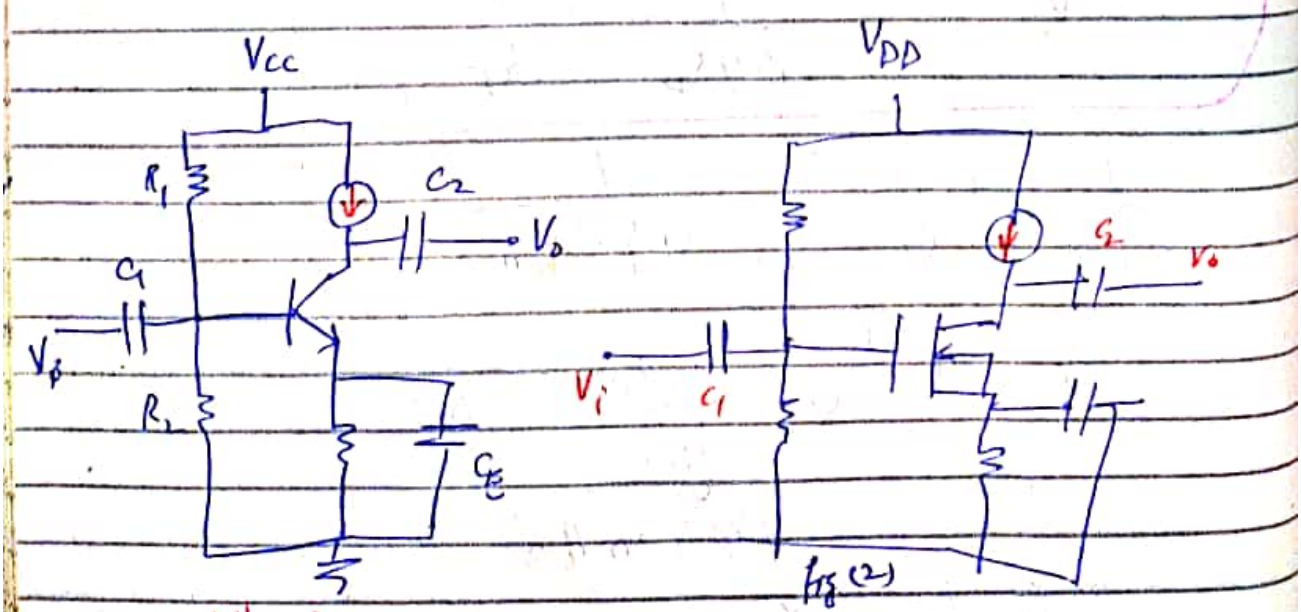
↳ C.S

R_D → FET amplifier } current source.
R_C → BJT amplifier }
↳ C.E

It is very difficult to realize value of particular resistance.

In ICs we use C.S and C.E amplifier.
↳ amplifier.

with constant current source as a load.
↳ in place of R_D or R_C.



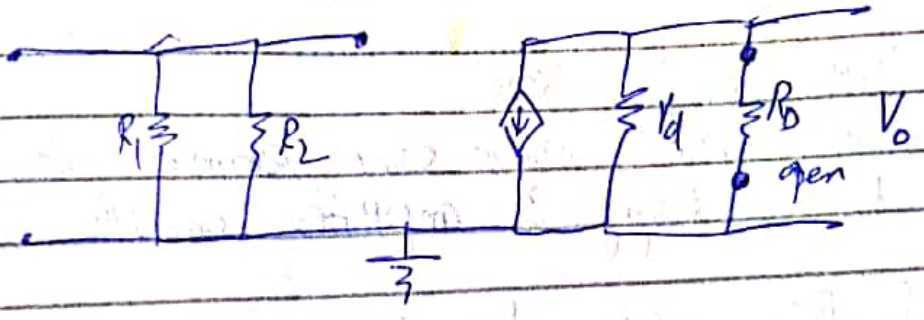
Why?

- It is much easier to create sources which are implemented using transistors.
  Bc values of resistors are very

difficult to realize and implement resistive values precisely.

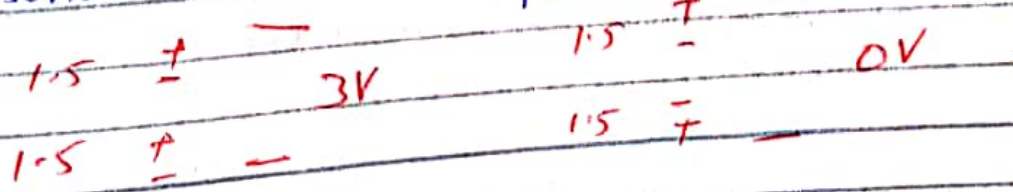
- Using Curr source because it provides a very high (ideally infinite) resistance and thus we obtain a much higher gain. Thus a finite R_D or R_C is used.

The AC eq circuit for fig 2 is as;

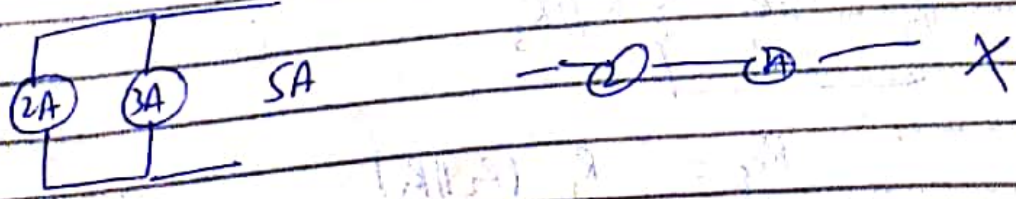


Current sources are connected in parallel.
Voltage " " " in series.

Two voltage sources connected in parallel →
The larger one feeds the smaller.
↳ In series → both have effect on the load.



Ideal voltage source has zero internal resistance.
" current " " infinite " "



A load is something that draws current from the source.
→ appliances

All resistors are connected in parallel → so equivalent resistance decreases → and hence current increases → power increases → bill increases

- The behaviour of device in saturation region is like a current source.

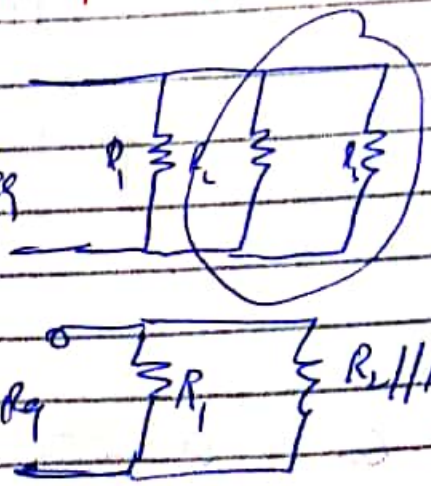
- Three configurations
  - common drain, common source, common gate
    - and accordingly 3 amplifier circuits.
  - for BJT, common base, common emitter, common collector.

common source → 180° phase shift.

common drain → source follower → impedence matching Buffer

common collector → emitter follower ↑

→ high i/p impedance and low output impedance.

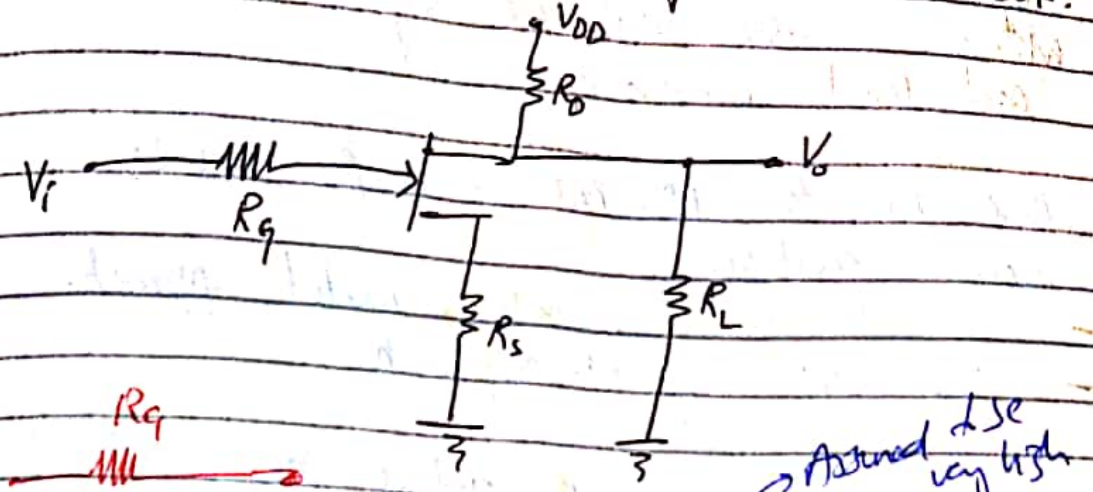


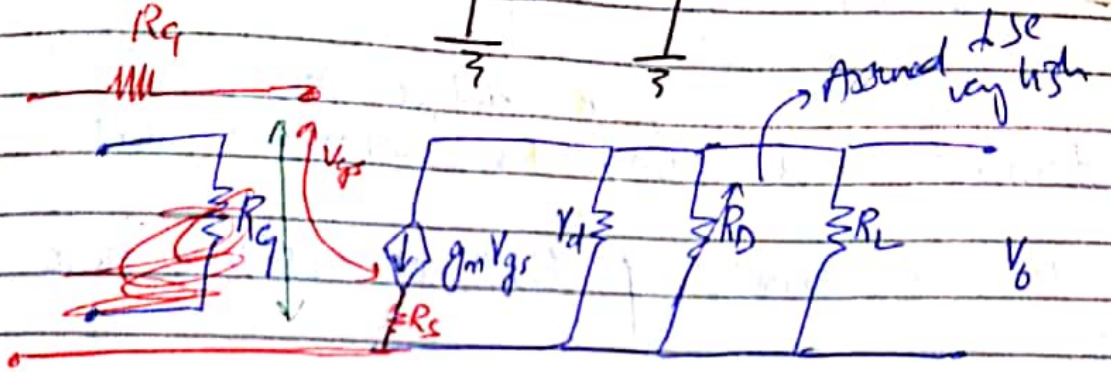
for two resistors

$$R_{eq} = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_{eq} = \frac{R_1 (R_2 \| R_3)}{R_1 + (R_2 \| R_3)}$$

Q: Determine the voltage gain in the circuit.





$$V_o = -g_m V_{gs} (R_D \| R_L)$$

$V_{gs} = ?$

$$V_G = V_{GS} + V_S$$

$$V_i = V_{gs} + g_m V_{gs} R_s$$

$$V_{gs} = \frac{V_i}{1 + g_m R_s}$$

$$V_o = -g_m \left(\frac{V_i}{1 + g_m R_s} \right) (R_D \| R_L)$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m (R_D \| R_L)}{1 + g_m R_s}$$

$Z_i = \infty$ $Z_o = R_D$

R_L is the load → say speaker
↳ resistance in ohms.

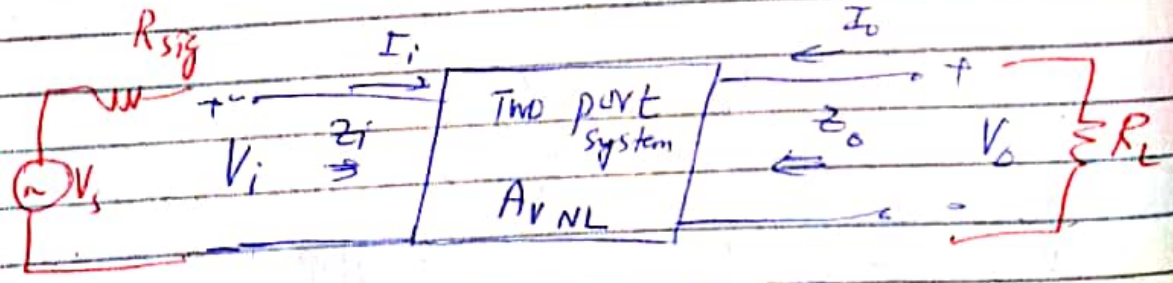
≥ M K Ω.

Uptill now we have determined Z_i, Z_o, A_v without considering the signal source resistance and load resistance.

There are two approaches to perform small signal analysis-
- Small signal equivalent model approach.
- Two port system approach
  - ↳ In this case, we analyze the circuit at terminal level rather than component level.

The same formulas of BJT are applicable here for FETs.

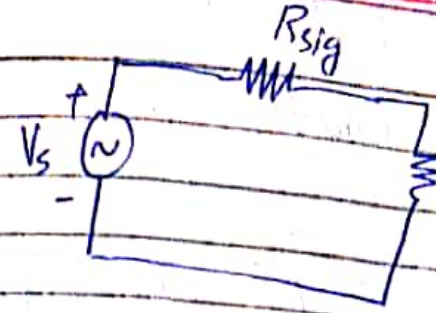
Three voltage gains.
- Voltage gain with no load. → maximum
- Voltage gain with load.
- Overall voltage gain



$$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{NL}} \qquad A_{v_{NL}} = \frac{V_o}{V_i}$$

$$A_{i_L} = -A_{v_L} \frac{Z_i}{R_L}$$

$$A_{v_s} = \frac{V_o}{V_s} \times \frac{V_i}{V_i}$$



$$V_i = \frac{R_i V_s}{R_i + R_{sig}}$$

$$\frac{V_i}{V_s} = \frac{R_i}{R_i + R_{sig}}$$

$$A_{Vs} = \left(\frac{R_i}{R_i + R_{sig}}\right)\left(\frac{R_l}{R_L + R_o}\right) A_{V_{NL}}$$

$A_{V_{NL}} > A_{V_L} > A_{V_s}$ → s/w gate tuned at drain sense circuit

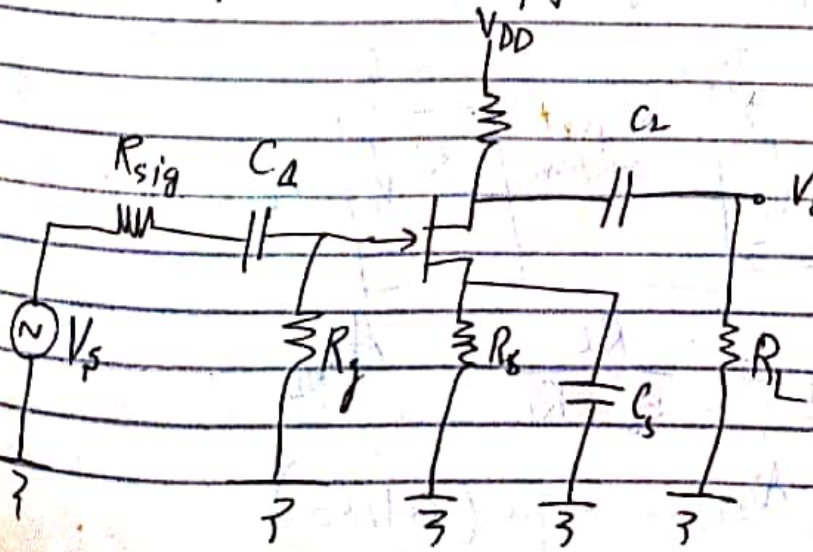
Due to high i/p impedance of FETs source impedance doesn't effect the output impedance.

O/P impedance is not effected by applied load.

High resistance provides safety for FET.
↳ not true for BJT.

Z_o doesn't include R_L.

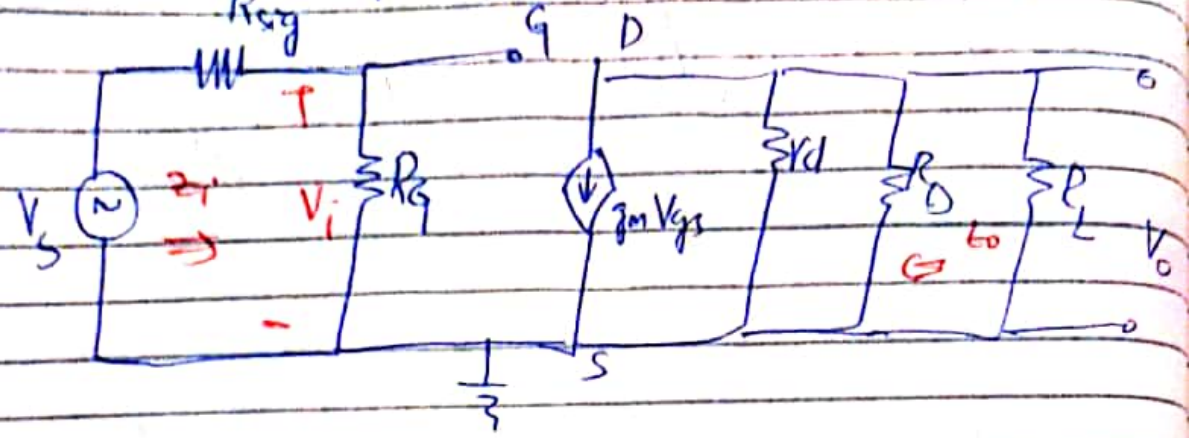
Self Bias Configuration.



$$A_{VS} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} \qquad \frac{V_i}{V_s} = \frac{R_G}{R_s + R_{sig}}$$

$$A_{VS} = -g_m \left(\frac{R_{sig}}{R_s + R_{sig}}\right) (r_d \,||\, R_D \,||\, R_L)$$

The small signal AC eq. circuit;



$$Z_i = R_G \qquad Z_o = r_d \,||\, R_D$$

$$V_o = -g_m V_{gs} (r_d \,||\, R_D \,||\, R_L)$$

A_{VL} doesn't include the effect of V_s & R_{sig}

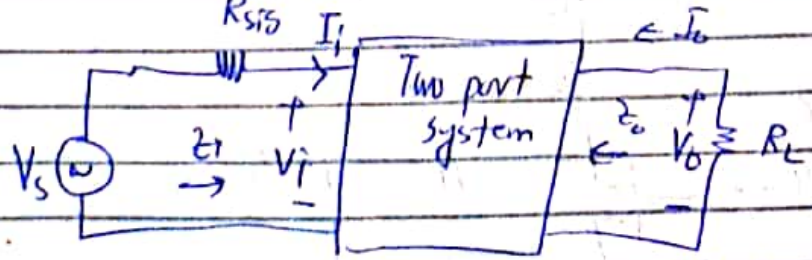
$V_i = V_{gs}$

$$V_o = -g_m V_i (r_d \,||\, R_D \,||\, R_L)$$

$$A_{VL} = -g_m (r_d \,||\, R_D \,||\, R_L)$$

$$A_{VNL} = -g_m (r_d \,||\, R_D)$$

By two port system approach



$$A_{VL} = \frac{R_L}{R_o + R_L} A_{VNL}$$

$$A_{VNL} = -g_m (r_d \,||\, R_D)$$

In sub (I) & (II)

$$A_{VL} = \frac{-g_m R_L (r_d \| R_D)}{r_d \| R_D + R_L} = -g_m (r_d \| R_D \| R_L)$$

$$A_{VS} = \frac{V_o}{V_s} = \left(\frac{V_o}{V_i}\right) \times \left(\frac{V_i}{V_s}\right)$$

$\hookrightarrow A_{VL}$ $\hookrightarrow$ for f_3.

$$\frac{V_i}{V_s} = \frac{R_i}{R_i + R_{sig}}$$

$R_i = R_G$ → internal component.

$$A_V = \frac{-g_m (R_D \| R_L)}{1 + g_m R_S}$$ → exact equation

r_d is very large.

$g_m R_S \gg 1$.

$$A_{VL} \simeq \frac{-R_D \| R_L}{R_S} \Big|_{g_m R_S \gg 1}$$

$R_D > R_L$

$$A_{VL} \simeq -\frac{R_L}{R_S}$$

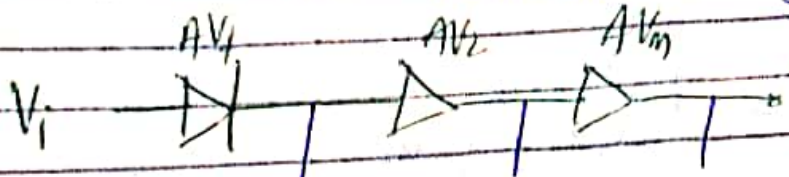
Cascaded system.

a I/P impedance of the second stage acts as load for the first stage.

(a) O/P impedance of the following stage acts as a load for the previous stage.

Why cascading?

To increase voltage gain



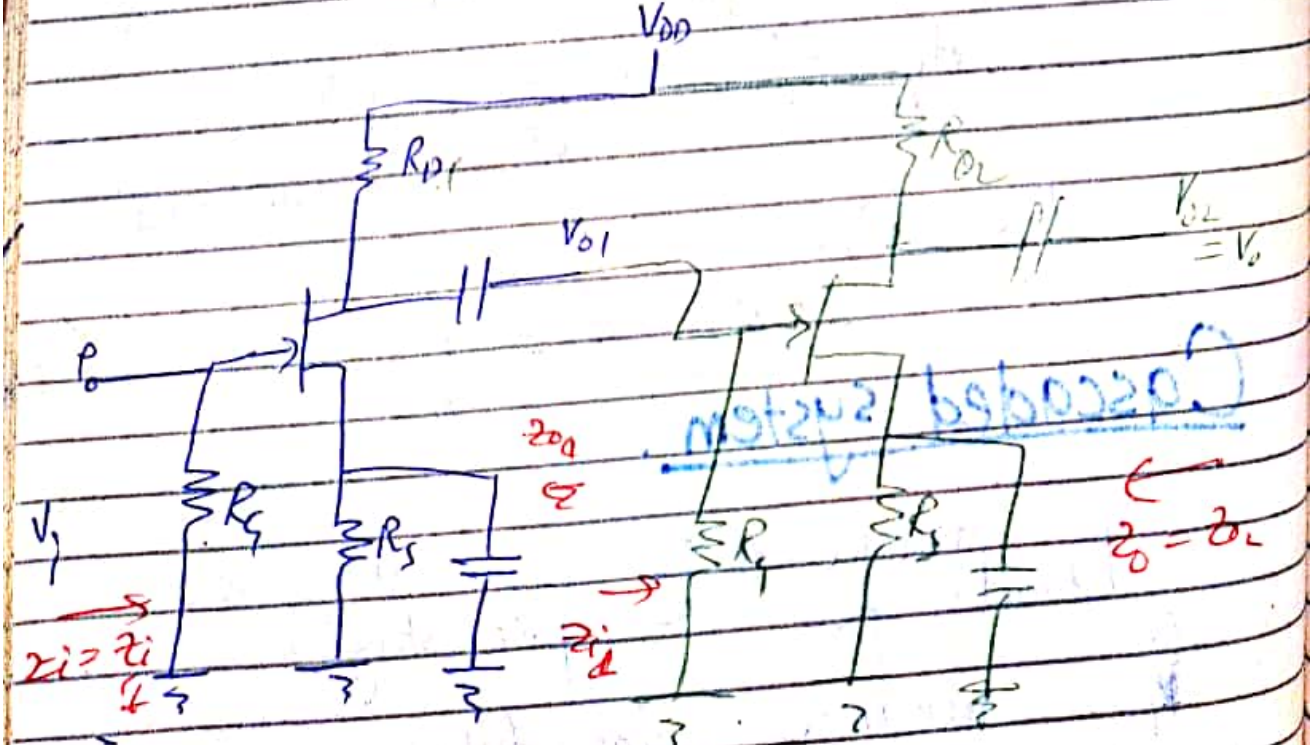
$$V_o = A_{V_1} A_{V_2} A_{V_3} \cdots A_{V_n} V_i$$

$$\frac{V_o}{V_i} = A_{V_1} \cdot A_{V_2} \cdot A_{V_3} \cdots A_{V_n}$$

$$A_V = A_{V_1} \cdot A_{V_2} \cdot A_{V_3} \cdots A_{V_m}$$

$$A_V|_{dB} = 20 \log_{10} A_V$$

$$A_P|_{dB} = 10 \log_{10} A_V$$



$V_o = A_{V1} \times A_{V2} \times V_i$

$A_V = \frac{V_o}{V_i}$

$\Rightarrow A_V = A_{V1} \cdot A_{V2}$

$A_{V1} \simeq -g_{m1} R_{D1}$

$A_{V2} \simeq -g_{m2} R_{D2}$

$\Rightarrow A_V = g_{m1} g_{m2} R_{D1} R_{D2}$

↳ No phase shift.

DMOSFET and JFET used for amplification

EMOSFET used for switching.

Final

Chapter 10
Operational Amplifier (Op Amp)

operation → mathematical operations.
IC → 741
Vacum tube → Semiconductor → ICs

Very high gain differential amplifier with very high input impedance and low output impedance.

Ideal Xtics of Op Amp

$A_V \to \infty$ $\quad$ $\epsilon_i \to 0$ $\quad$ $Z_o \to 0$ $\quad$ BW → ∞

↓ Open loop voltage gain

By connecting external components we will obtain a fixed amount of gain.

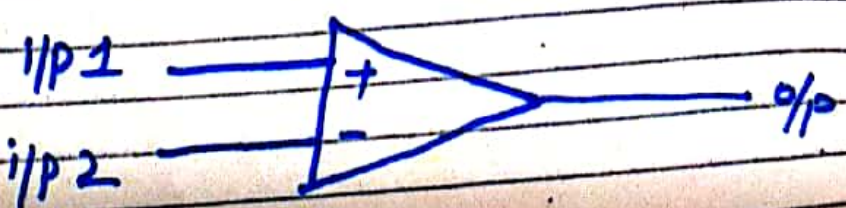
↓ reduce? reducing offset is nil

↓ reduce? impedance matching becomes easier.

↓ passes all frequencies from 0 to ∞

Uses?

- Voltage amplitude changes
- Oscillators.
- Filters
- many types of instrumentation circuits.

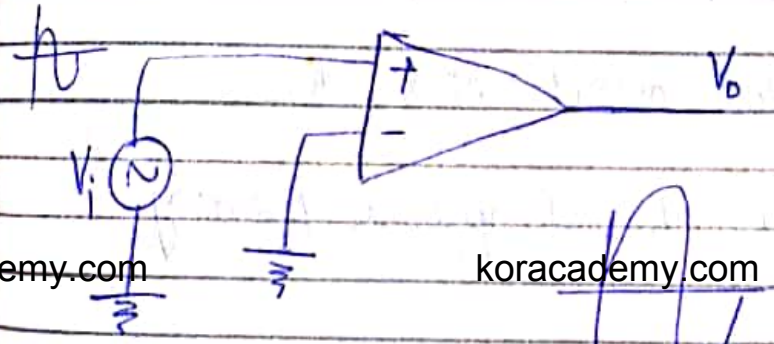


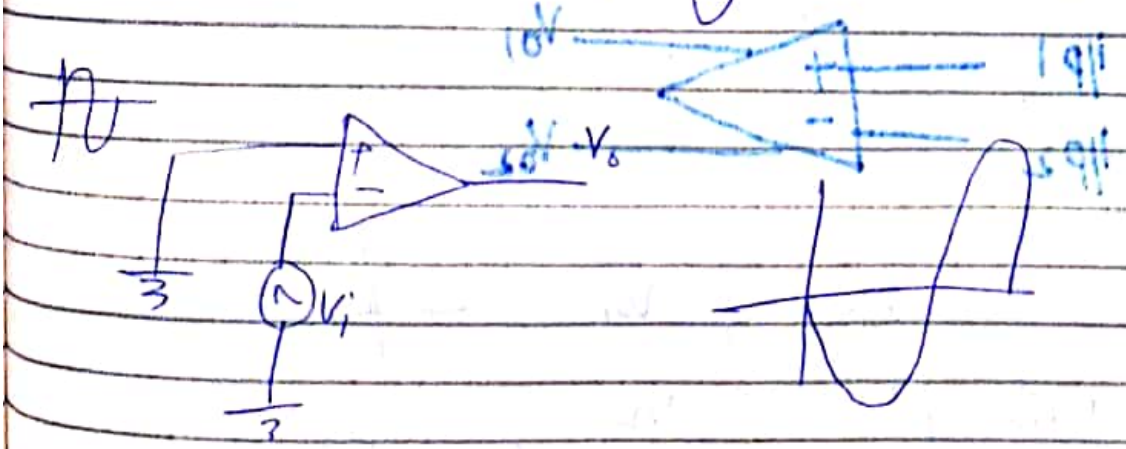
+ non inverting input.
− inverting input

↳ i/p and o/p are in phase.
↳ i/p and o/p are out of phase by 180°.

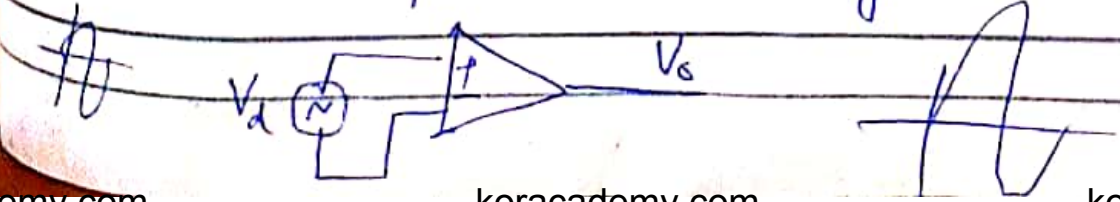
Modes of Operation.

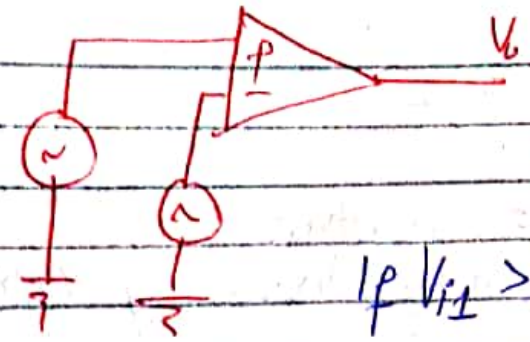
1- Single i/p ended operation.
↳ signal is applied at one of the input and the other i/p is grounded.





2- Double ended (differential) i/p operation
i/p is provided at both terminals and none of the terminal is grounded.



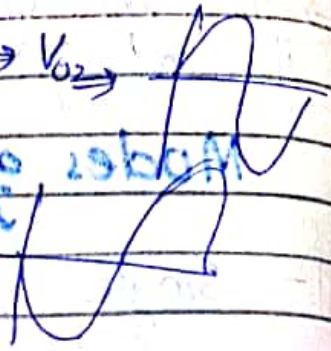


V_o

$V_o = V_{i1} - V_{i2}$

If $V_{i1} > V_{i2} \Rightarrow V_{o2}$

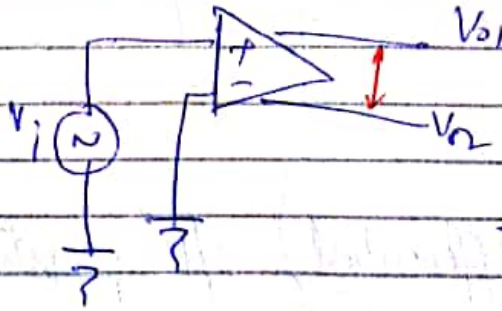
If $V_{i1} < V_{i2}$

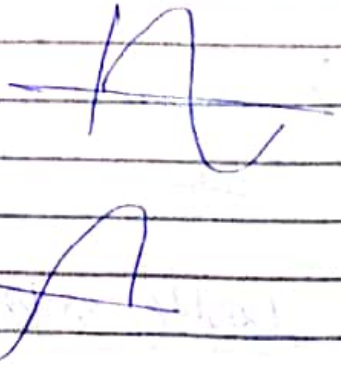


We can also have two outputs which be out of phase by 180°.

- Double ended output operation

one i/p → two o/ps of opposite polarity
two i/ps → " "





$V_o = V_{o1} - V_{o2}$

↳ difference output.

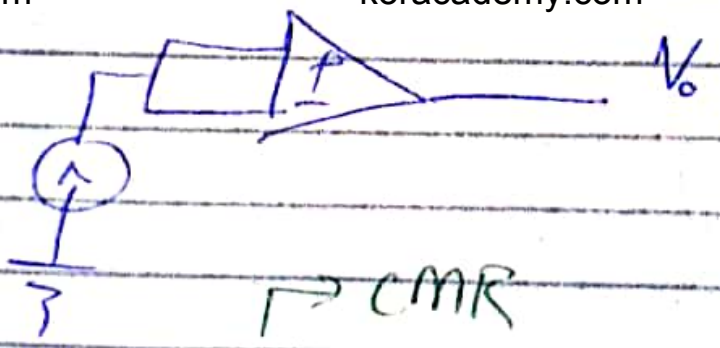
↳ floating signal

Both i/ps inverted.] → fully differential
both o/ps inverted] operation.

- Common Mode Operation.

When the same signal is applied at both inputs.

↳ Ideally o/p should be zero.
↳ But there is still a small output.



↳ CMR

common mode rejection → differential amplifier should amplify the difference signal and reject the common mode signal (eg noise)

$$CMRR = \frac{A_d}{A_c}$$ Ideally ∞.

Date: / /

FINAL

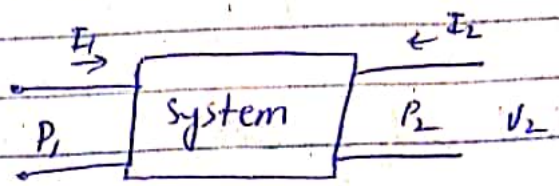
Lecture 1.

dB, dBW, dBm, dBV

↳ decibel

$P_1 \rightarrow$ i/p power.
$V_1 \rightarrow$ i/p voltage
$I_1 \rightarrow$ i/p current

$P_2 \rightarrow$ o/p power.
$V_2 \rightarrow$ o/p voltage.
$I_2 \rightarrow$ o/p current.



System may be an amplifier circuit.

$$1 \text{ bel} = \log_{10} \frac{P_2}{P_1}$$

$1 \text{ bel} = 10 \text{ dB}$

$$\text{No. of dBs} = 10 \log \frac{P_2}{P_1}$$

where $\frac{P_2}{P_1}$ is the power gain (A_p).

→ If the power gain is 10 dB, the o/p power is 10 times input power.

$\log_{\text{base}} \text{base} = 1$

Positive dB indicates gain and negative indicates loss.

eg $P_1 = 100W$ $P_2 = 1000W$ $\Rightarrow$ $A_p = 10 \text{ dB}$.

→ If $P_1 = 100W$ $P_2 = 10W$ $\Rightarrow$ $A_p = \frac{1}{10} = 0.1$

Also $A_p = 10 \log 0.1 = 10 \log_{10} 10^{-1} = -10 \text{ dB}$

↳ loss.

Bilal Register

If A_p is -10dB, o/p P is 10 times smaller than i/p power.

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A_p of an amplifier circuit is 10dB. $P_1 = 10W$

$P_2 = 10 \times 10 = 100W$

If A_p is 3dB, o/p power is twice that of the i/p power. $\Rightarrow P_2 = 2P_1$

If A_p is -3dB, o/p is half of i/p power.

$P_2 = \frac{1}{2} P_1$

eg $A_p = 3dB$, $P_2 = 60W$ $P_1 = ?$

$P_2 = 2P_1 \Rightarrow P_1 = \frac{P_2}{2} = 30W$

eg $A_p = -3dB$, $P_2 = 60W$ $P_1 = ?$

$P_2 = \frac{1}{2} P_1 \Rightarrow P_1 = 2P_2 = 120W$

→ If we are given ~~simple~~ single power ? In that case we use dBW or dBm.

dBW → decibel watt ↓ Reference power is 1W.

$P|_{dBW} = 10 \log \frac{P}{1W}$

dBm → dB milliwatt ↓ Reference power is 1mW.

$P|_{dBm} = 10 \log \frac{P}{1mW}$

eg Express P = 100W in dBm and dBW.

$P|_{dBm} = 10 \log \frac{P}{1mW} = 10 \log \frac{100W}{1mW}$

$= 10 \log \frac{100 \times 1000 mW}{1mW}$

Bilal Register

Date: / /

$10 \log_{10} 10^5 = 10 \times 5 \log_{10} 10 = 50 dBm$

$\Rightarrow P|_{dBW} = 10 \log_{10} \frac{P}{1W} = 10 \log \frac{100W}{1W}$

$= 20 dBW$

$P|_{dBm} = P|_{dBW} + 30$

$P|_{dBW} = P|_{dBm} - 30$

Voltage Gain in dB ?

We assume that i/p and o/p resistance are of 1Ω.

$R_1 = R_2 = 1\Omega$

Three expressions for Power;

$P = VI$, $P = \frac{V^2}{R}$, $P = I^2R$

$A_P = 10 \log_{10} \frac{P_2}{P_1} = 10 \log \frac{V_2^2/R_2}{V_1^2/R_1}$

$A_V = 10 \log \left(\frac{V_2}{V_1}\right)^2 = 20 \log \left(\frac{V_2}{V_1}\right)$

$A_P = 3dB \Rightarrow A_V = 6dB$

$P_2 = 2P_1$ $V_2 = 2V_1$

Date: / /

If one voltage is given → taken reference 1V.

$$|V|_{dBV} = 20 \log \frac{V}{1V}$$

↳ reference

Current Gain in dB

$$A_p = 10 \log_{10}\left(\frac{P_2}{P_1}\right) = 10 \log \left(\frac{I_2^2 R}{I_1^2 R}\right)$$

$$= 10 \log \left(\frac{I_2}{I_1}\right)^2$$

$$\boxed{|A_I|_{dB} = 20 \log_{10}\left(\frac{I_2}{I_1}\right)}$$

Negative voltage gain indicates phase reversal.

Negative power gain indicates power loss.

↳ In cascaded systems, the gains are multiplied
↳ similarly in dBs also

$$|A_v|_{dB} = 20 \log_{10} A_v = 20 \log_{10}(A_{v_1} A_{v_2})$$

$$= 20 \log_{10} A_{v_1} + 20 \log_{10} A_{v_2} \text{ ....}$$

Date: / /

CMRR

Common Mode Rejection Ratio.

↳ The ability of amplifier to amplify the difference (desired) signal and reject the common (unwanted) signal.

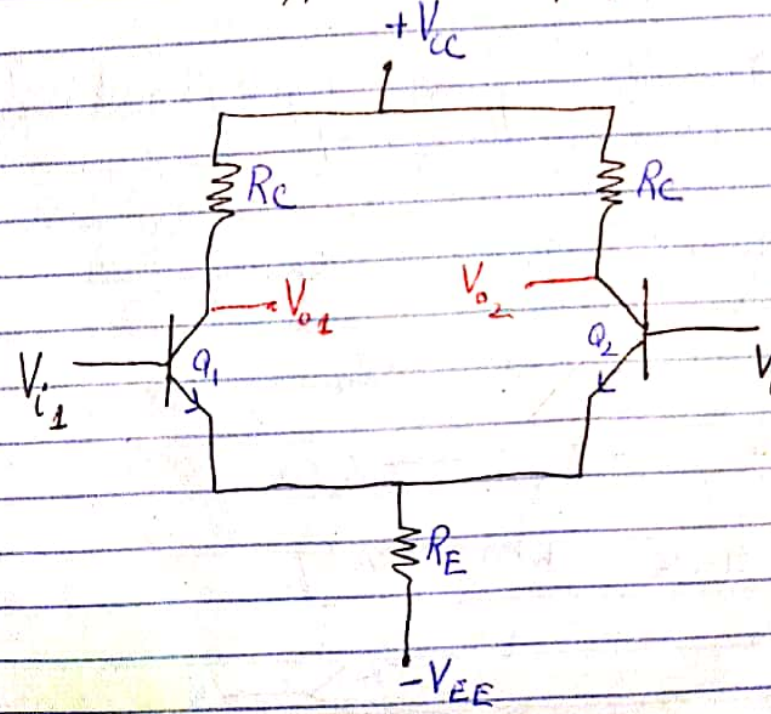
The fundamental unit (block) of op amp is differential amplifier. → cascaded with each other.
↳ resulting in a very high gain.

ch of ideal op Amp.

→ Open loop voltage gain is infinite.
→ I/p impedance is infinite.
→ o/p impedance is zero.
→ Bandwidth is infinite
↳ from DC to infinity → all pass.

→ popular connection used in integrated circuits.

A basic differential amplifier circuit is shown;



Bilal Register

Date: __/__/__

We assume that the two transistors are matched ie

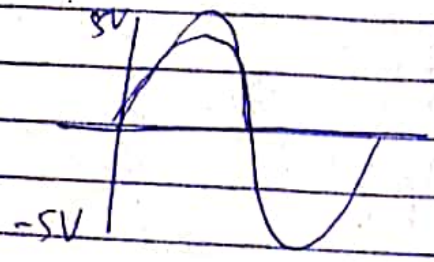
$V_{BE_1} = V_{BE_2} = V_{BE}$

$I_{B1} = I_{B2} = I_B$

$I_{C1} = I_{C2} = I_C$

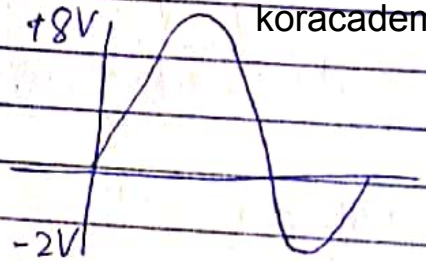
$I_{E1} = I_{E2} = I_E$

Q_1 and Q_2 are matched.



No offset

If we add +3V

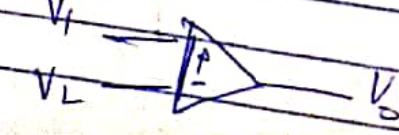


offset of 3V

When transistors are not properly matched, we will have a dc offset.

Symbol for the differential amplifier is as;

Don't confuse it with op amp



Bilal Register

Date: / /

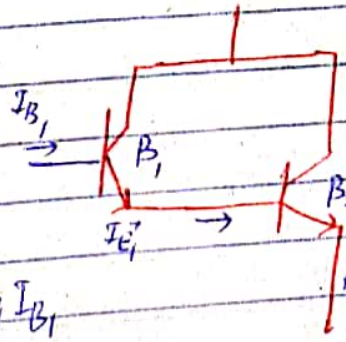
Apply signal at one terminal while the other I/P is grounded → single ended operation.

Double ended operation → Signals of opposite polarities are provided at both the I/P terminals.

Diff Amp amplifies difference of both the signals.

Common Mode operation → When the same signal is applied at both inputs.

Darlington pair is also called super β transistor.
↳ provides very high current gain.



$I_{E_1} = \beta_1 I_{B_1}$

$\beta_D = \beta_1 \beta_2$

$I_{E_2} = \beta_2 I_{E_1}$

$I_{E_2} = \beta_1 \beta_2 I_{B_1}$

$I_{E_2} = \beta_D I_{B_1}$

DC Analysis of Diff Amp Circuit

Capacitors are replaced by open circuit equivalent and AC sources are grounded.

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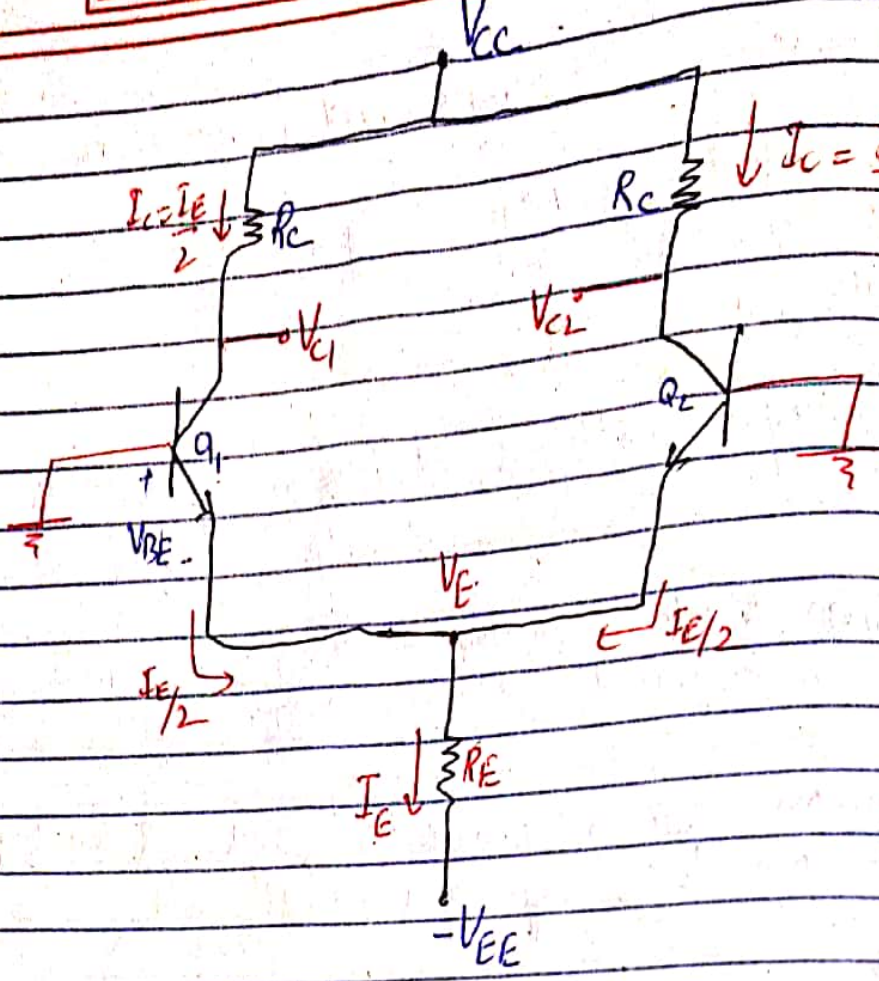


$V_E = V_{EB} + V_B$

$V_{BE} = -V_{EB} \Rightarrow V_{EB} = -V_{BE}$

$\Rightarrow V_E = -V_{BE} + V_B$

$V_B = 0V$

$\Rightarrow \boxed{V_E = -0.7V}$

$I_E = ?$ $\quad I_E = \frac{V_E - (-V_{EE})}{R_E} = \frac{V_E + V_{EE}}{R_E}$

$$\boxed{I_E = \frac{V_{EE} - 0.7}{R_E}}$$

Bilal Register

Date: / /

$I_C = ?$

$$I_{C1} = I_{C2} = I_C = \frac{I_E}{2}$$

$$\Rightarrow \boxed{I_C = \frac{V_{EE} - 0.7}{2R_E}}$$

$V_C = ?$

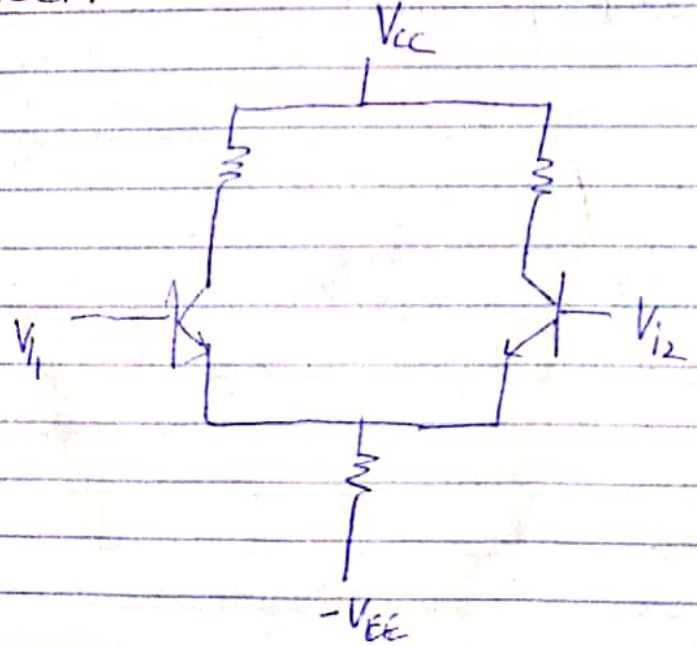
$$V_{C1} = V_{C2} = V_C = V_{CC} - I_C R_C = \frac{I_E}{2} R_C$$

$$\boxed{V_C = \frac{V_{EE} - 0.7}{2R_E} (R_C)}$$

DC analysis is performed to establish the Q point.

AC analysis of the Diff Amp Ckt.

Capacitors are short circuited and DC sources are grounded.



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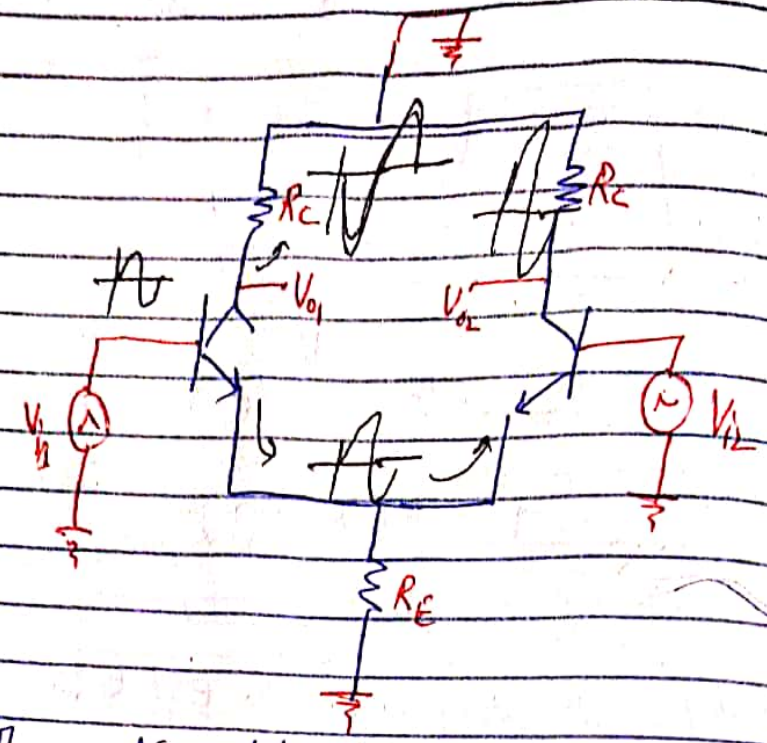
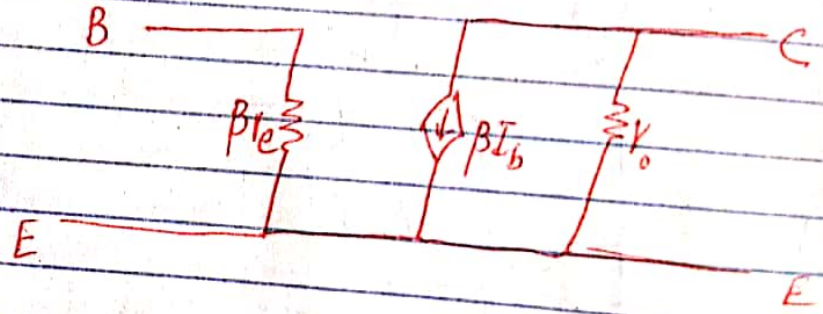
The AC equivalent circuit is,



Three AC models:
re model, hybrid, and hybrid π model.
↓
used for high frequency

The re model for common emitter amplifier circuit is as,



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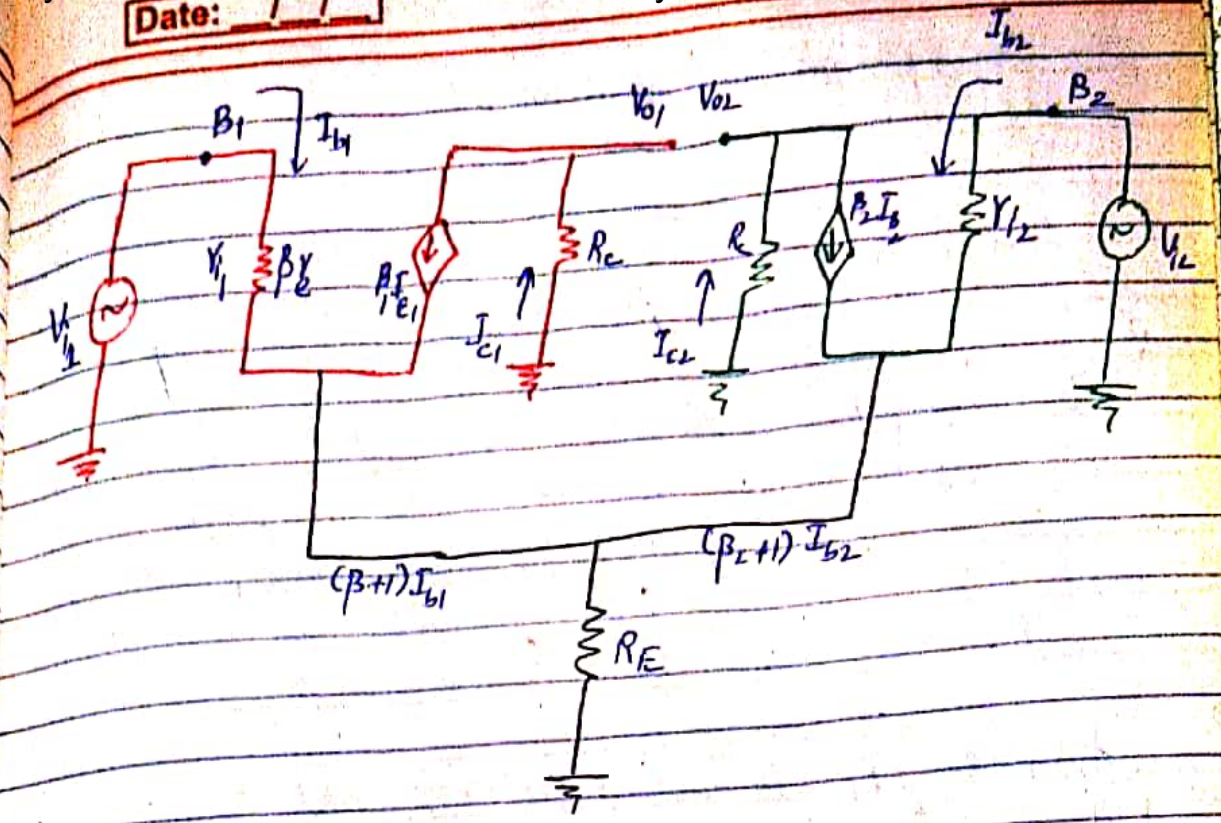


AC ckt

↳ Superposition theorem → one source at a time

→ say V_{i2} is grounded

↳ still we can take output from both transistors. → How?

signal is given at base of Q_1 → so o/p appears at collectors and emitter

↳ If o/p is taken from collector → CE

↳ If " " emitter → C.C

emitter is common → so the same signal appears at emitter of Q_2 → I/p → base is grounded

o/p from collector ← C.B

V_{o1} and V_{o2} will be out of phase by 180° as shown in figure.

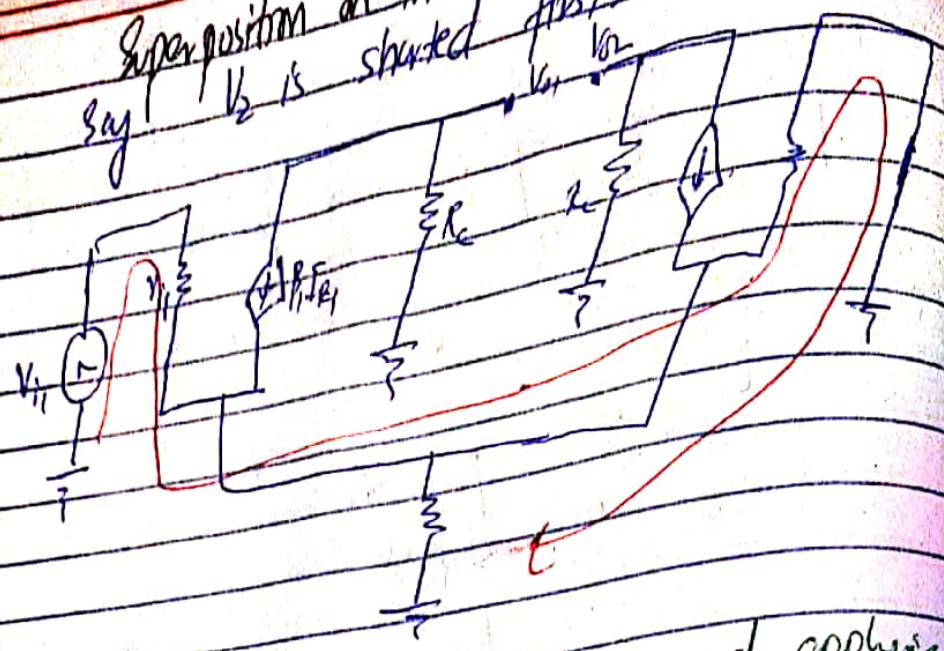
↳ Similarly if Q_2 is grounded.

Q_2 → C.E, C.C Q_1 → C.B

Bilal Register

Date: / /

Superposition on the re model;
Say V_2 is shorted first.



Assuming R_E to be very large and applying KVL to the loop

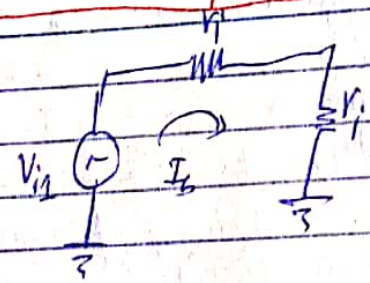
$-V_{i1} + I_{b1} r_i + I_{b1} \beta r_e = 0$

$I_{b1} = I_{b2} = I_b$

$r_i = r_{i1} = r_{i2} = \beta r_e$

$\beta_1 = \beta_2 = \beta$

$$I_b = \frac{V_{i1}}{2r_i} = \frac{V_i}{2\beta r_e}$$



$$I_b = \frac{V_{i1}}{2r_i} = \frac{V_{i1}}{2\beta r_e}$$

$$I_c = \beta I_B = \frac{\beta V_i}{2\beta r_e} \qquad I_c = \frac{V_i}{2r_e}$$

$V_o = ?$ $\quad V_o = I_c R_c = \frac{V_i}{2r_e} R_c$

$$\frac{V_o}{V_i} = \frac{R_c}{2r_e} \qquad A_v = \frac{R_c}{2r_e}$$

→ single ended with high gain available at either collector.

Bilal Register

Date: / /

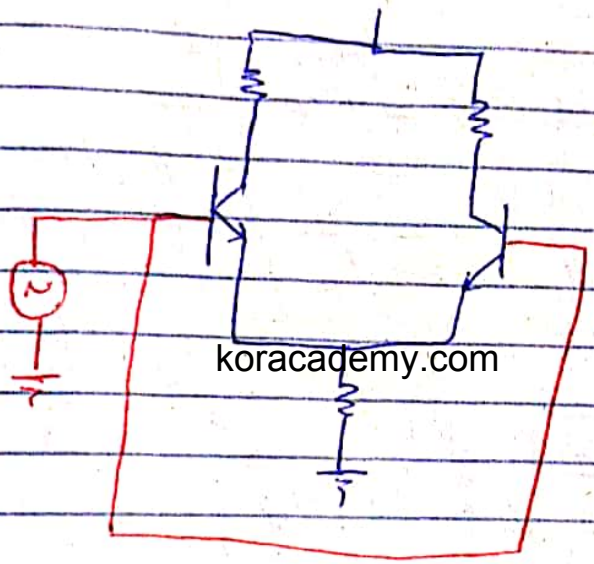
The double ended voltage gain is twice the single ended.

$$\frac{V_o}{V_d} = A_d = \frac{R_c}{r_e}$$

A_d → differential voltage gain.

V_d → difference signal $= V_{i_1} - V_{i_2}$

Now **Common Mode Operation**

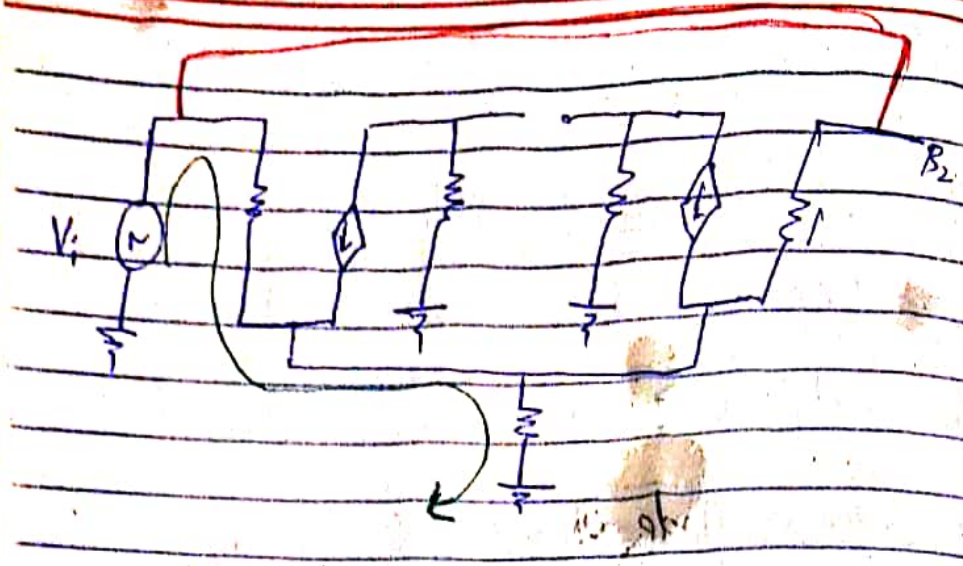


Ideally o/p should be zero for common mode operation
↳ So gain is zero. ↳ A_c

$$CMRR = \frac{A_d}{A_c}$$ Ideally infinite

The re model for common mode is shown on the next page.

Date: / /



Apply KVL to the loop.

$$-V_i + I_b r_i + 2(\beta+1) I_b R_E = 0$$

$$I_b = \frac{V_i}{r_i + 2(\beta+1)R_E}$$

$$I_C = \beta I_b$$

$$V_o = I_C R_C$$

$$V_o = \beta I_b R_C = \frac{\beta V_i R_C}{V_i + 2(\beta+1)R_E}$$

Voltage gain

$$\frac{V_o}{V_i} = \frac{\beta R_C}{V_i + 2(\beta+1)R_E} = A_C$$

A_C common mode gain.

Application of Diff Amp → in ICs

R_E is large ← problem

↳ requires larger area

↳ Replace by current source

↳ has infinite ideal resistance

Fig 10.20 and 10.21

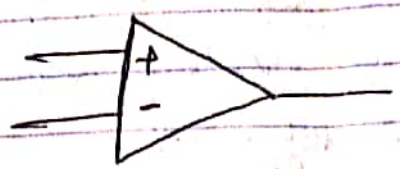
Bilal Register

Date: / /

Op-Amp Basics

→ i/p impedance in mega ohms
→ o/p " less than 100 ohms.
→ very high gain differential amplifier.
→ open loop gain is in range 10^5 to 10^6.

Symbol



+ → non inverting input — → inverting input

o/p and i/p are in phase

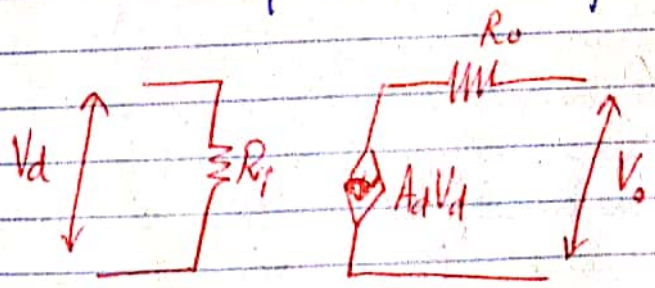
i/p and o/p are out of phase by 180°.

Xtics of ideal op-amp

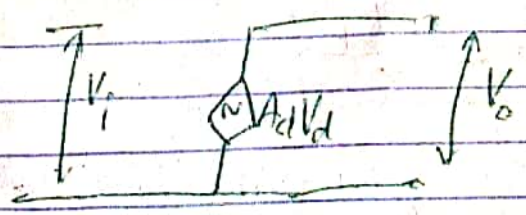
$A_v \to \infty$ open loop gain $R_i \to \infty$

$BW \to \infty$ $R_o \to 0$

The ac equivalent circuit of op-amp is as; (practical)



Ideally



Bilal Register

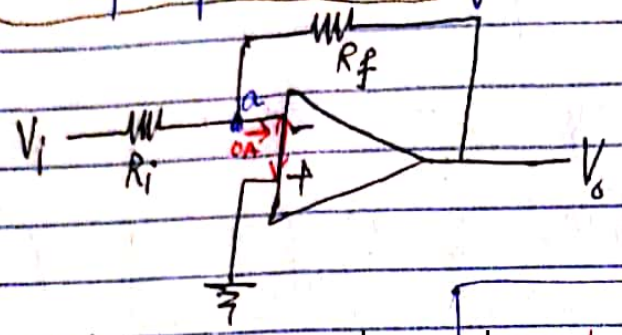
Date: / /

Virtual ground → physically does not exist but helps in the analysis of circuit.

Inverting Amplifier

is any amplifier circuit that gives o/p that is 180° out of phase w.r.t inputs.

(i) i/p C.S in FET, C.E in BJT
(ii) op amp in inverting mode.



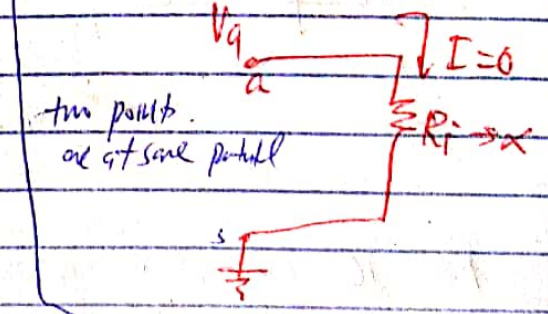
OA b/c R_i is infinite.

Node a

KCL assuming that all currents are leaving the node

$$\frac{V_a - V_i}{R_i} + \frac{V_a - V_o}{R_f} = 0$$

Virtual ground / virtual short



$\therefore V_a = 0$

$$-\frac{V_i}{R_i} - \frac{V_o}{R_f} = 0 \qquad \frac{V_o}{R_f} = -\frac{V_i}{R_i}$$

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

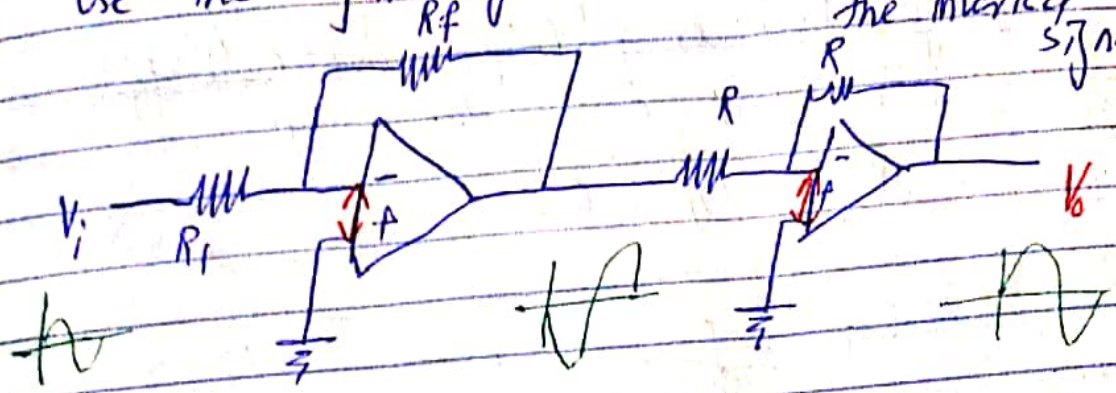
↳ closed loop gain → now is constant → depending on R_f and R_i

Bilal Register

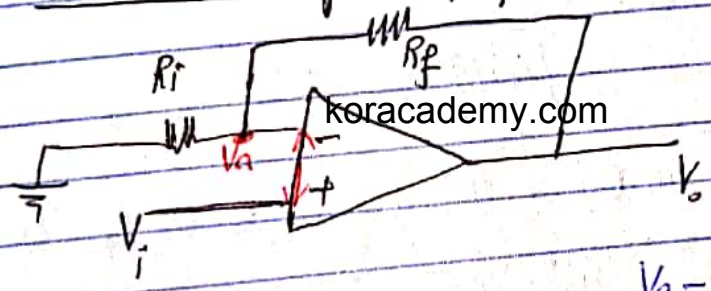
Date: / /

If you just want to invert the signal and not amplify it → put $R_f = R_i$

If you want to first amplify then invert → use the following circuit



Non Inverting Amplifier



Node → no current entering or leaving.

$$\frac{V_a - 0}{R_i} + \frac{V_a - V_o}{R_f} = 0$$

Virtual short $\Rightarrow V_i = V_a$

$$\frac{V_i}{R_i} + \frac{V_i - V_o}{R_f} = 0$$

$$\frac{V_i}{R_i} + \frac{V_i}{R_f} - \frac{V_o}{R_f} = 0$$

$$V_i \left(\frac{1}{R_i} + \frac{1}{R_f} \right) = \frac{V_o}{R_f}$$

$$V_i \left(\frac{R_i + R_f}{R_i R_f} \right) = \frac{V_o}{R_f}$$

Date: / /

$\frac{V_o}{V_i} = \frac{R_i}{R_i} + \frac{R_f}{R_i}$ i/p and o/p are in phase.

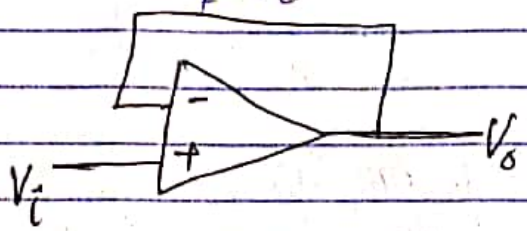
$$\rightarrow A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$$

Voltage Follower / Unity Follower / Buffer

To make gain equal to unity

make $R_i = \infty$ → exactly

$i_f \rightarrow 0$

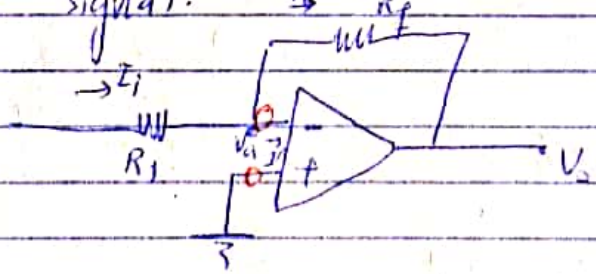


$A_V = 1$

$V_o = V_i$

Lecture 2 ~~2/12/19~~

Diff amp → amplifies the difference of the input signal.



$Z_i = R_i$

Ideal op Amp X tics

$A_{OL} \rightarrow \infty$ $R_i \rightarrow \infty$ $R_o \rightarrow 0$ $BW \rightarrow \infty$

Current flows through actual ground and not through virtual ground.

$I_i = I_f + I^{\nearrow 0}$

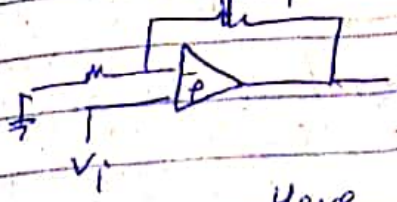
$\frac{V_i - V_a^{\nearrow 0}}{R_1} = \frac{V_a - V_o}{R_f}$ $\frac{V_i}{R_i} = \frac{-V_o}{R_f}$

Bilal Register

Date: / /

$$\Rightarrow \boxed{A_{CL} = \frac{V_o}{V_i} = \frac{-R_f}{R_i}}$$

Similarly for non inverting amplifier.



$$A_{CL} = 1 + \frac{R_f}{R_i}$$

Here $Z_i = \infty$

In BJT common collector provides a gain less than 1. ↳ emitter follower.

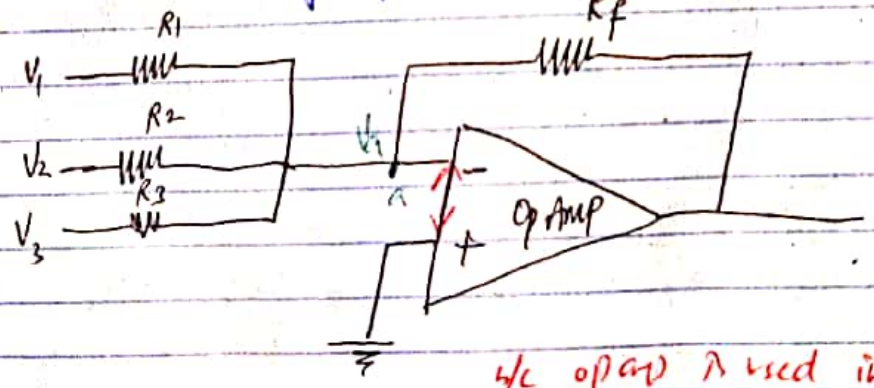
in FET Sarce follower provides voltage gain less than 1. ↳ common dram

absander → تابع / مزود

Summing Amplifier

→ Op Amp can also be used to provide algebric sum of inputs. with a separate gain factor. ↓ multiple

→ For each input, there is a separate gain multiplier.



w/c opamp is used in inverting mode

Also called inverting summing amplifier.

Virtual ground. KCL to hide a

$$\frac{V_a - V_1}{R_1} + \frac{V_a - V_2}{R_2} + \frac{V_a - V_3}{R_3} + \frac{V_a - V_o}{R_f} = 0$$

Bilal Register

Date: / /

$V_a = 0$

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

$\frac{R_f}{R_n}$ → constant gain multiplier / scale factor for the nth input.

If $R_f = R_1 = R_2 = R_3$

$$\Rightarrow V_o = -(V_1 + V_2 + V_3)$$

Here we have shown only three inputs, we can also have more.

Example $V_1 = +1V \quad V_2 = +2V \quad V_3 = +3V$

$R_1 = 500\,k\Omega \quad R_2 = 1M\Omega = R_3 = R_f = 1M\Omega$

$$V_o = -\left(\frac{1M\Omega}{500K}(1) + \frac{1M\Omega}{1M\Omega}(2) + \frac{1M\Omega}{1M\Omega}(3)\right)$$

$$V_o = -7$$

Example

$V_1 = -2V \quad V_2 = +3V \quad V_3 = +1V$

$R_1 = 200\,k\Omega \quad R_2 = 500\,k\Omega \quad R_3 = R_f = 1M\Omega$

$$V_o = -\left(\frac{1M\Omega}{200K}(-2) + \frac{1M\Omega}{500K}(3) + \frac{1M\Omega}{1M\Omega}(1)\right)$$

$$V_o = +3V$$

Bilal Register

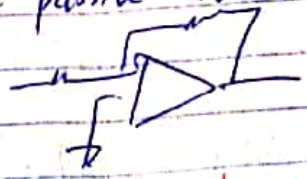
Date: / /

Integrator can act as a low pass filter.

Integrator.

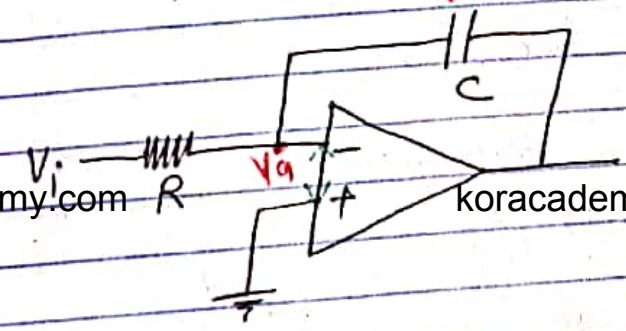
$V_i \rightarrow$ [Integrator] $\rightarrow V_o = \int V_i\,dt$

Both i/p and feedback are passive and resistive element in op amp.



In inverting amplifier, if we replace feedback resistor by a capacitor → the resulting circuit is called integrator.

o/p is integration of i/p with inversion.



i/p element → resistive
feedback elemt → capacitive

$$I_C = C\frac{dV}{dt}$$

KCL at node a using the concept of virtual ground.

$$\frac{V_a - V_i}{R} + C\frac{d(V_a - V_o)}{dt} = 0$$

$V_a = 0$

$$-\frac{V_i}{R} - C\frac{dV_o}{dt} = 0$$

$$\Rightarrow \int dV_o = \int -\frac{1}{RC} V_i\,dt$$

Integrate

$$\boxed{V_o = -\frac{1}{RC}\int V_i\,dt}$$

Gain factor $= \frac{1}{RC}$

$\Rightarrow V_o \propto -\int V_i\,dt$

Bilal Register

Date: __/__/__

Unit of RC is second.

$$RC = \frac{V}{I} \times \frac{\Omega}{V} \Rightarrow RC = sec$$

(or) $\tau = RC = \frac{\Omega}{\Omega} \times F = \frac{\Omega}{\Omega} \frac{V}{A} \times \frac{A}{V} \times s$

$$RC = sec$$

Integrator circuit is used in analog computations.
Can be used to solve differential equations.

Integrator provides the ability to solve electrical analogues of physical problems.
↳ It provides continuous summation.

Integration is a linear operation.
↳ $\int (V_1 + V_2)\,dt = \int V_1\,dt + \int V_2\,dt$

The gain of this amplifier circuit is $-\frac{X_C}{R}$.

$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C}$ ↳ gain $= -\frac{1}{2\pi f RC}$

At DC this amplifier circuit will behave just like an open loop.
↳ the gain becomes infinite → open loop gain.

Integrator is a low pass filter b/c as frequency increases, gain reduces.
At a certain time, some frequency will be blocked.

Bilal Register

Date: / /

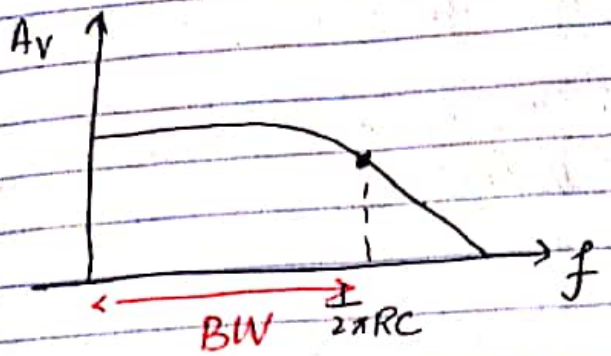
For wtt off frequency

$2\pi fRC = 1$

$\Rightarrow f = \frac{1}{2\pi RC}$

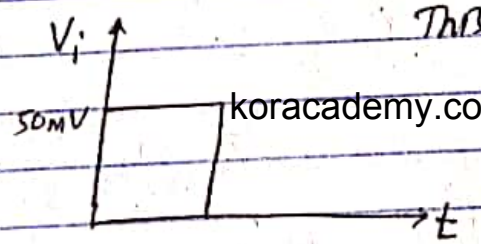
Half power point

↳ At this frequency o/p power is half of i/p pwr.
↳ -3dB
↓
In terms of A_v, this point is -6dB



We can also apply multiple inputs → then it will be called summing integrator.

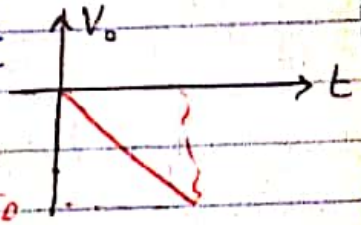
Example



This signal is applied to integrator with R = 1mΩ
C = 1μF.

$\frac{1}{RC} = \frac{1}{1\times10^{-6}\times10^{6}\times1} = 1$

$V_o = -\frac{1}{RC}\int V_i\,dt = -50\times10^{-3}\,t$



If i/p is constant → o/p is ramp
If i/p is ramp → o/p is square

For opamp amplifier → If we try to increase the o/p than the power supply → the device will be in saturation mode.

As $\frac{1}{RC}$ increases, slope of o/p increases → it becomes more steeper.

Bilal Register

Date: / /

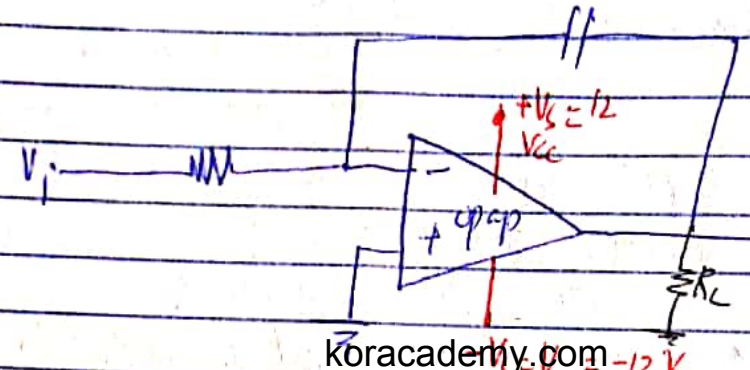
Example $V_i = V_m = 50mV$ $t = 1s$ is applied to Mt amp.

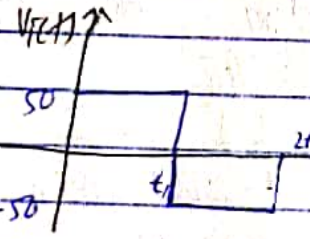
The ckt parameter of amp are $R_f = 100k\Omega$, $C = 0.1\mu F$, supply voltages are $+V_s$ and $-V_s = 12$

The initial voltage / charge on capacitor is zero.

(i) Calculate the o/p voltage $V_o(t)$.

(ii) Plot $V_o(t)$ vs time.





$V_c(0) = 0 \Rightarrow V_o(0) = 0$

$V_i(t) = 50mV \quad 0 \le t < 1$

$V_i(t) = -50mV \quad 1 \le t < 2$

$$V_o(t) - V_o(t_i) = -\frac{1}{RC}\int_{t_i}^{t} V_i(t)\,dt$$

For the first time interval. ie 0 to 1.

$$V_o(t) - V_o(0) = -\frac{1}{0.1 \times 100 \times 10^3 \times 10^{-6}}\int_0^t (50 \times 10^{-3})\,dt$$

$$= -5\Big|_0^t \Rightarrow \boxed{V_o(t) = -5t}$$

$\hookrightarrow 0 \le t < 1$

Bilal Register

Now the voltage across capacitor will become the initial voltage for the next case.
ie at $t = 1s$

Now for second time interval $1 \le t < 2$

At $t = t_1 = 1s$

$V_0(t) = V_0(t_1) = V_0(1) = -5V$

↓

initial voltage across capacitor. ie the initial o/p voltage for -ve half cycle of i/p voltage

$$V_0(t) - V_0(t_1) = -\frac{1}{RC}\int_{t_1}^{t} V_i(t)\,dt$$

$t_1 = 1s \quad V_0(t_1) = -5V$

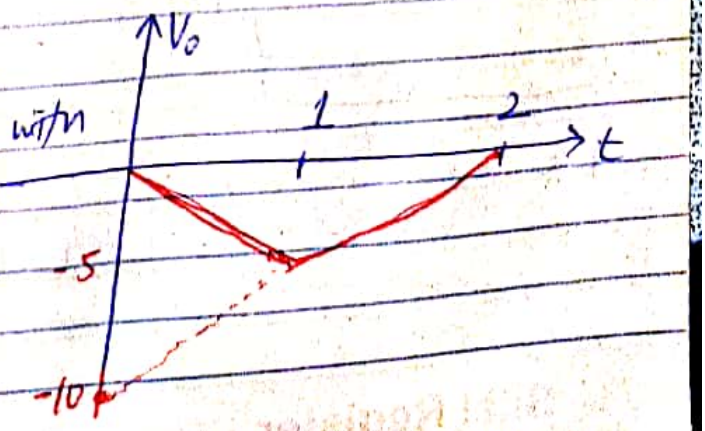
$$V_0(t) - (-5V) = -\frac{1}{100\times10^{3}\times0.1\times10^{-6}}\int_{1}^{t} -50\times10^{-3}\,dt$$

$$V_0(t) + 5 = 5t - 5$$

$$\boxed{V_0(t) = 5t - 10} \quad \text{for } 1 \le t < 2$$

(when we put $t=2$ here, it becomes zero.

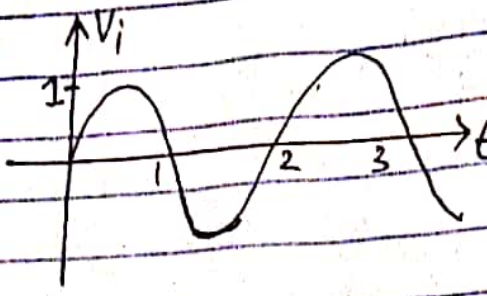
-10 → y intercept.
→ I/p is periodic wave form with period 2s → so o/p will be periodic with period 2s.



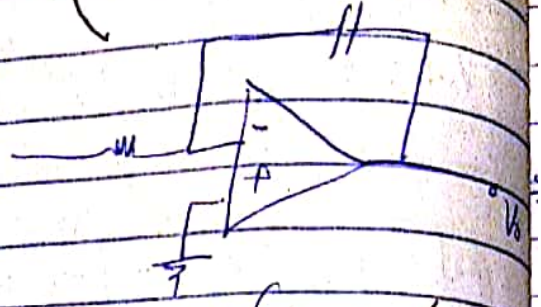
Bilal Register

Date: / /

⇒ Apply a sinuside at the input of Integrator and plot the output waveform.



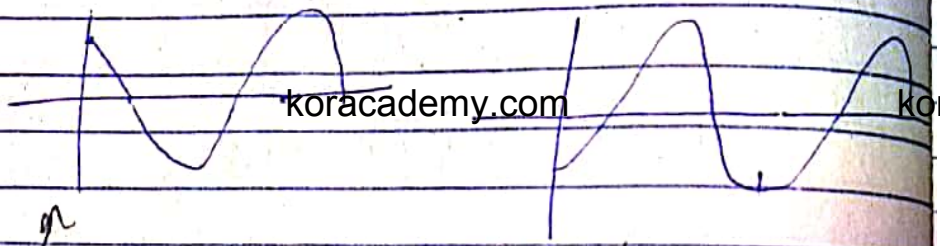
Time period is 2s.



$$V_o(t) = \frac{-1}{RC}\int V_i(t)\,dt$$

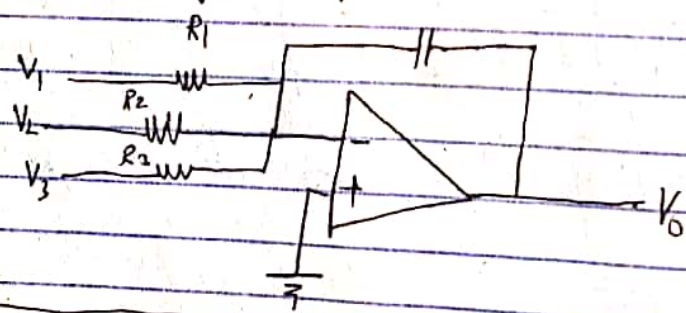
$$= -\frac{1}{RC}\int V_m \sin\omega t\,dt = -\frac{1}{RC}(-\cos\omega t)$$

$$= \frac{1}{RC}\cos\omega t$$



This question is assignment.

Summing Integrator



$$V_o = -\left(\frac{1}{R_1C}\int V_1\,dt + \frac{1}{R_2C}\int V_2\,dt + \frac{1}{R_3C}\int V_3\,dt\right)$$

Bilal Register

Date: / /

Summing integrator finds its application in analog computations.

C → feedback element R_1, R_2, R_3 → I/p resistive elements.

↓

reactive component

↳ -ve feedback phenomena.

↳ Helps solving differential equations electrically.

Example $C = 1\mu F$ $R_1 = 200\,k\Omega$ $R_2 = 100\,k\Omega$

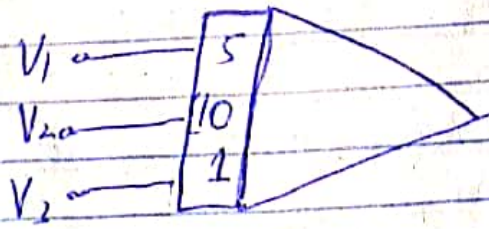
$R_3 = 1M\Omega$

$$\frac{1}{R_1 C} = \frac{1}{200 \times 10^3 \times 1 \times 10^{-6}} = 5$$

$$\frac{1}{R_2 C} = \frac{1}{100 \times 10^3 \times 1 \times 10^{-6}} = 10$$

$$\frac{1}{R_3 C} = \frac{1}{1 \times 10^6 \times 1 \times 10^{-6}} = 1$$

Analogue computation representation of three input summing integrator.



↳ This symbol just shows the scale factors.

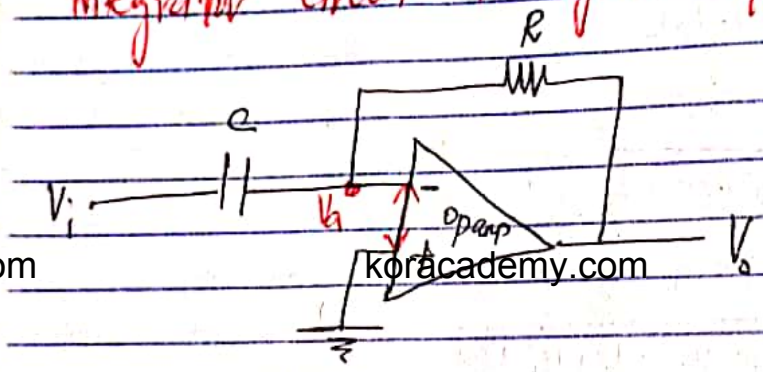
Date: / /

Differentiator

V_1 → Differential Amplifier ← V_2 → $V_o = A(V_1 - V_2)$

V_i → Differentiator → $V_o = \frac{dV_i}{dt}$

Swap the positions of R and C in the integrator circuit to get differentiator.



Apply KCL to node a and applying the concept of virtual ground.

$$C\frac{d}{dt}(V_a - V_i) + \frac{V_a - V_o}{R} = 0$$

$V_a = 0$

$$V_o = -RC\frac{dV_i}{dt}$$

So differentiator provides two operations;

1- Differentiation
2- Amplitude reversal

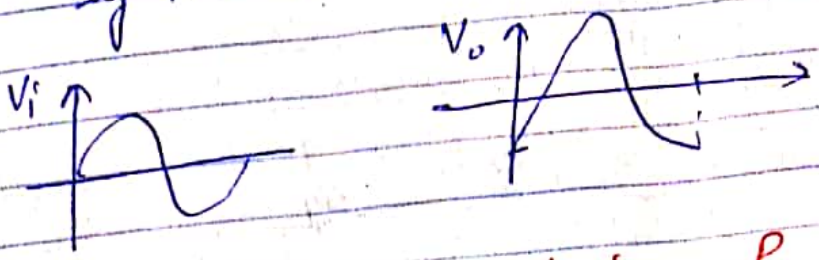
Bilal Register

Date: / /

eg $V_i = \sin \omega t$

$$V_o = -RC \frac{d}{dt} \sin \omega t$$

say $RC = 1 \Rightarrow V_o = -\omega \cos \omega t$

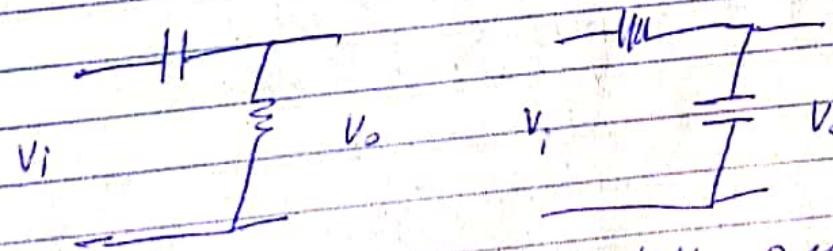


The gain of this circuit is $\frac{-R}{X_c} = -R\omega C$

$= -2\pi f RC$

$\therefore f \uparrow \Rightarrow$ gain $\uparrow$

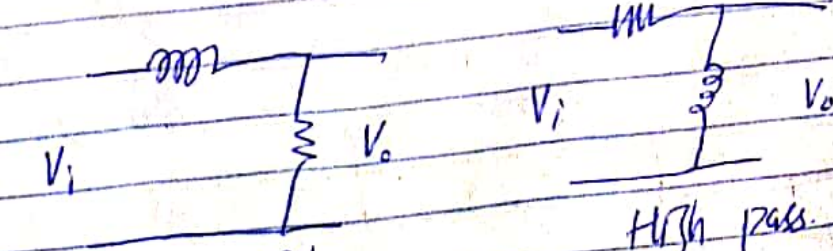
$\Rightarrow$ differentiator is a high pass filter.



High pass filter

Low pass

$X_c = \frac{1}{2\pi f C}$ $X_c \downarrow f \uparrow$



Low pass filter

High pass

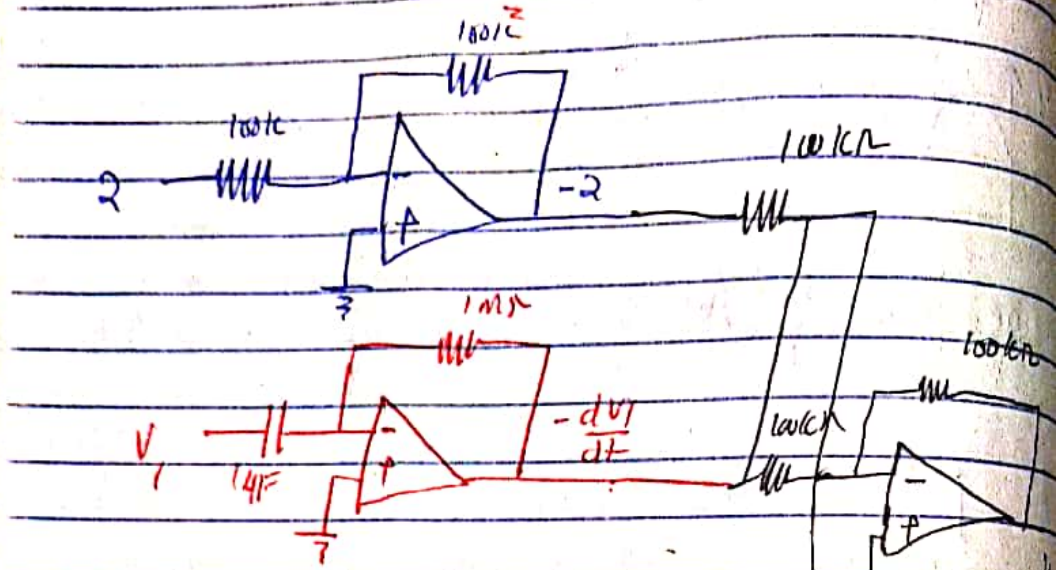
$X_L = 2\pi f L$ $X_L \uparrow f \uparrow$

Bilal Register

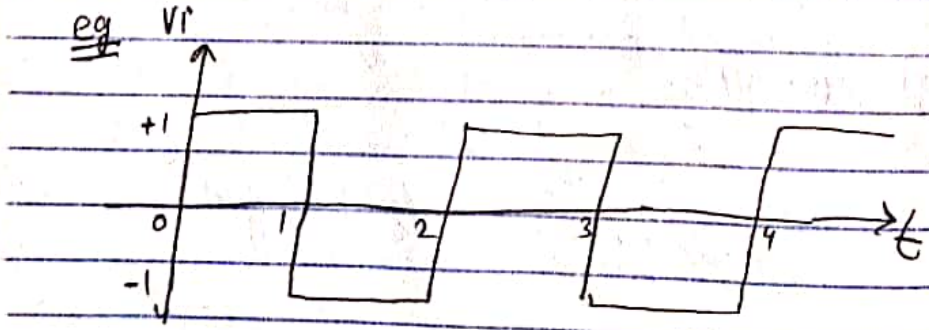
Date: / /

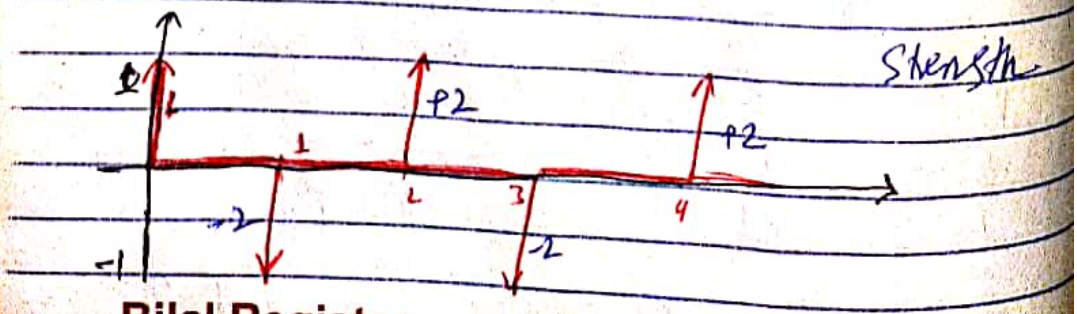
Reactance → opposition to AC.

let $V_o = 2 + \frac{dV_1}{dt} - \int V_2 \, dt$



eg





Bilal Register

Date: 1/1

Arrow → spike → impulse function

offset voltage

↳ strength / weight → depends on jump

↳ downward to upward → +ve

↳ up to down → -ve

Fourier series is used for the spectral representation of sinusoidal signals.

Cos θ even function → y-axis

↳ symmetrical w.r.t vertical axis.

Sin is odd function.

Lecture 3

09/10/19

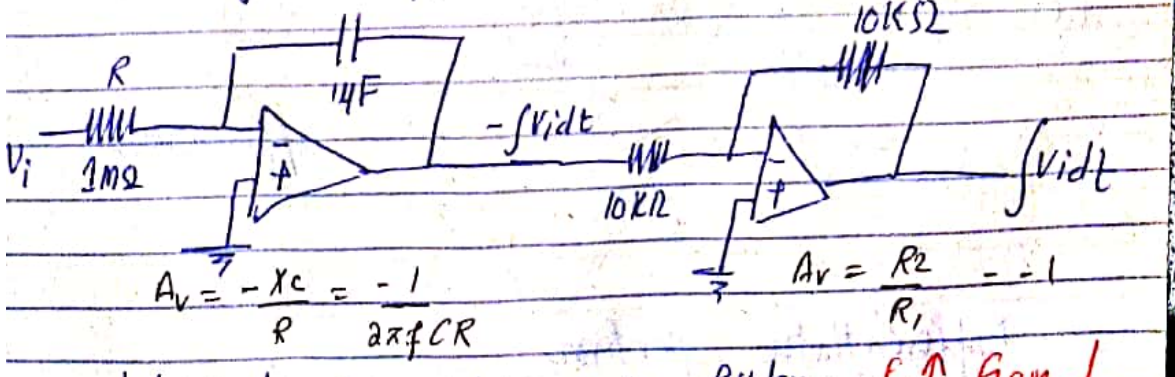
Develop circuit for the following equation.

$$V_o = \int V_i \, dt$$

The o/p of integrator is $V_o = -\frac{1}{RC}\int V_i dt$

Make $RC = 1$.

To remove -ve sign, pass it through another inverting amplifier with unity gain.

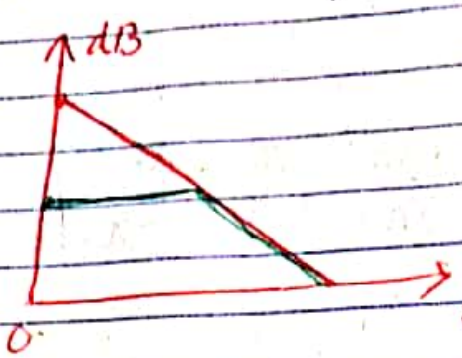


Integrator is a low pass filter. f ↑ Gain ↓

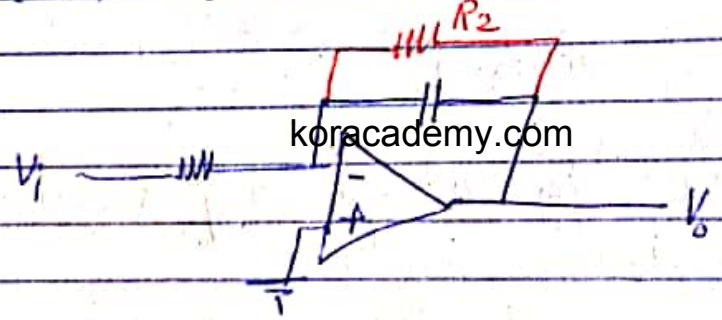
Bilal Register

Date: __/__/__

At DC gain is maximum.
As frequency increases ; gain reduces
↳ just like an open circuit → open loop
↳ Gain will be open loop gain.



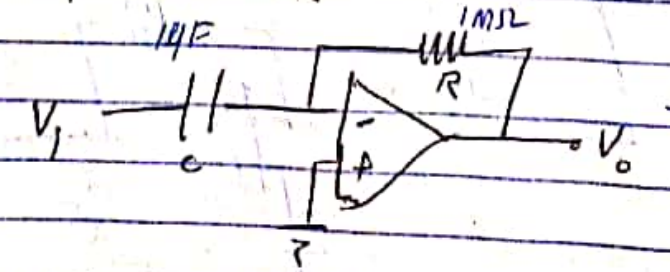
To avoid saturation (open loop operation), we place a resistor R_2 as shown.



Now by installing R_2, the gain becomes as shown.

$f \uparrow \Rightarrow X_c \downarrow, A_v \downarrow$

Let $V_i = 5 \cos(2\pi \times 60)t$



→ Differentiator

Differentiator performs
(i) Differentiation (ii) Amplitude phase reversal.

Bilal Register

For differentiator, $V_o = -RC \frac{dV_i}{dt}$

$= -1 \times 10^6 \times 10^{-6} \frac{d}{dt}(5\cos(2\pi \times 60)t)$

$= -5 \times 2\pi \times 60(-\sin(2\pi \times 60)t)$

$= 10\pi \times 60(\sin 2\pi 60t)$

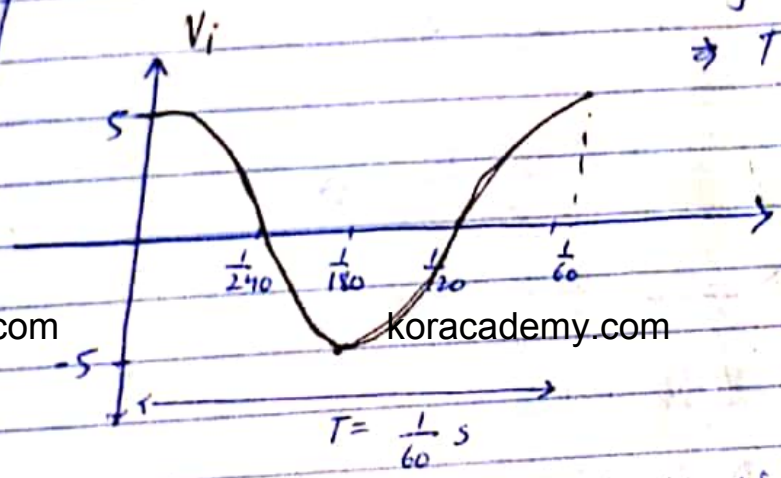
$= 600\pi \sin(2\pi 60t)$

As $\omega = 2\pi f$

$2\pi 60 = 2\pi f$

$f = 60$ Hz

$\Rightarrow T = \frac{1}{60}$ sec.



$V_p = 5V$

$V_{p-p} = 10V$

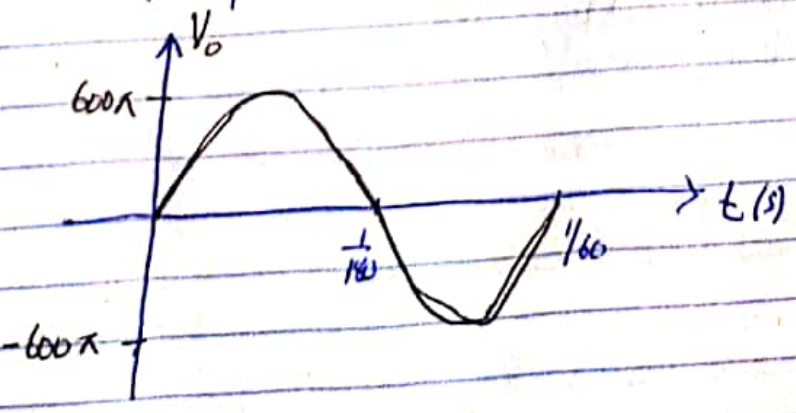
$V_{rms} = \frac{V_p}{\sqrt{2}}$

Both cos and sine are sinusoidal functions but with a phase shift of 90°.

Sin laggs, Cos leads

$\sin \omega t = \cos(\omega t - 90°)$, $\cos \omega t = \sin(\omega t + 90°)$

For o/p period is the same.



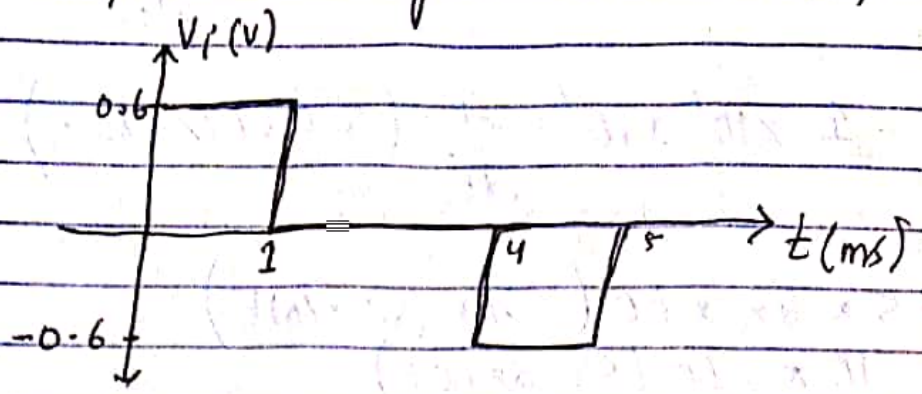
$V_p = 600\pi$ V

$V_{p-p} = 1200\pi$ V

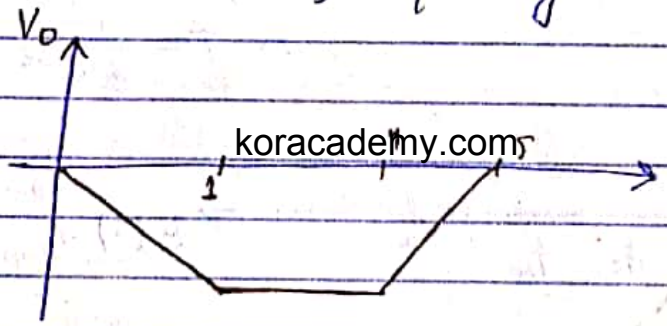
Bilal Register

Date: __/__/__

→ Input to integrator is as shown;



For the +ve pulse → -ve ramp
No signal → capacitor retains previous voltage
-ve pulse → increases till the next pulse.
↳ change polarity



Why $\frac{1}{RC}$? slope

$\frac{1}{RC}$ ↑ ⇒ ↑ slope

$\frac{1}{RC}$ ↓ ⇒ ↓ slope

Whenever a fixed voltage is applied to integrator, the output is a ramp.

Date: / / Chapter 14

Feedback and Oscillator Circuits:

Feedback → take some part of output and apply it at the input.

- -ve — How -ve or +ve ? Depends on the relative polarity of the signal being fed back to the circuit. → w.r.t input signal.
- +ve

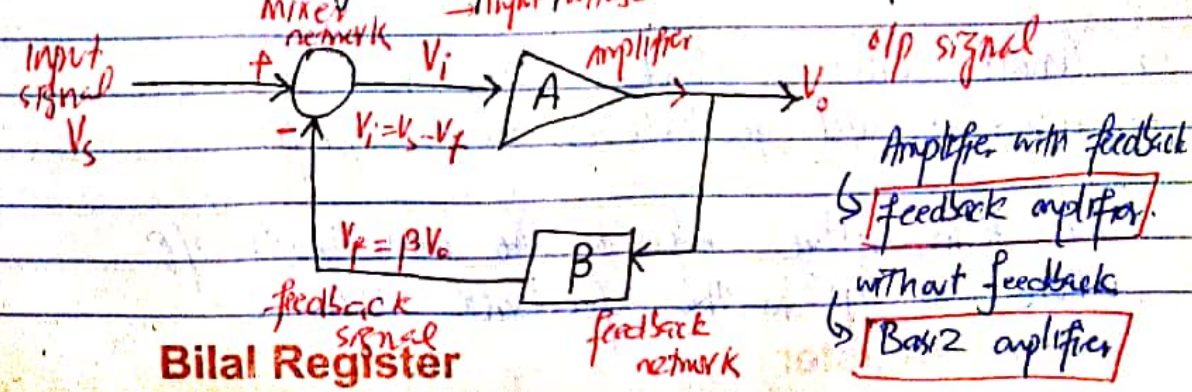
If polarity of o/p is +ve w.r.t i/p → +ve feedback
" " " -ve w.r.t i/p → -ve " .

-ve feedback reduces the overall voltage gain but improves other features of the circuit.

- -ve feedback phenomena is used in amplifier ckts.
- +ve feedback phenomena is used in oscillator ckts.

- i/p impedance increases.
- o/p impedance reduces.
- Better stabilized voltage gain.
- Frequency response improved.
- Noise is reduced.
- More linear operations.

Block diagram of feedback amplifier.



Bilal Register

Date: __/__/__

β will determine the portion of o/p to be provided at i/p in feedback.

→ Voltage is sensed in parallel.
→ Current is sensed in series.

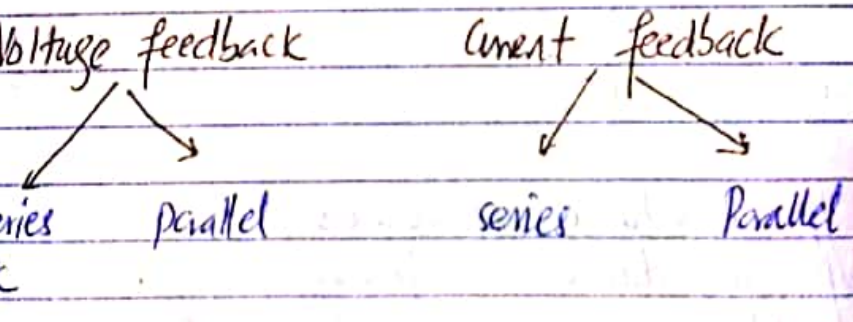
Currents are subtracted in parallel.
Voltages are subtracted in series.

β is called feedback factor or feedback ratio.

Feedback Connection types

Two types.

(i) Parallel / shunt feedback.
(ii) Series feedback.



→ The amplifier that uses voltage series feedback phenomena is called voltage amplifier.
→ That uses voltage shunt feedback → trans resistance amplifier.

→ Current series feedback → trans conductance amplifier
→ Current parallel feedback → current amplifier.

The term voltage refers to connecting the i/p voltage as i/p to the feedback network.

Bilal Register

Date: / /

The terms "current" refers to tapping off some o/p current through the feedback network.

The term "series" refers to connecting the feedback signal in series with the i/p voltage signal. (V_s).

The term "shunt" refers to connecting the feedback signal in shunt /parallel with an i/p current sarce.

Series feedback connection increases the i/p impedance.
Shunt feedback " decreases " " "

Voltage feedback decreases the i/p impedance.
Current feedback increases the i/p impedance.

Typically high i/p and lower i/p impedances are desired for most cascaded amplifiers.

→ So voltage series feedback connection is prefenced.

Voltage Series Feedback Connection

also called

Here all quantities are voltages.

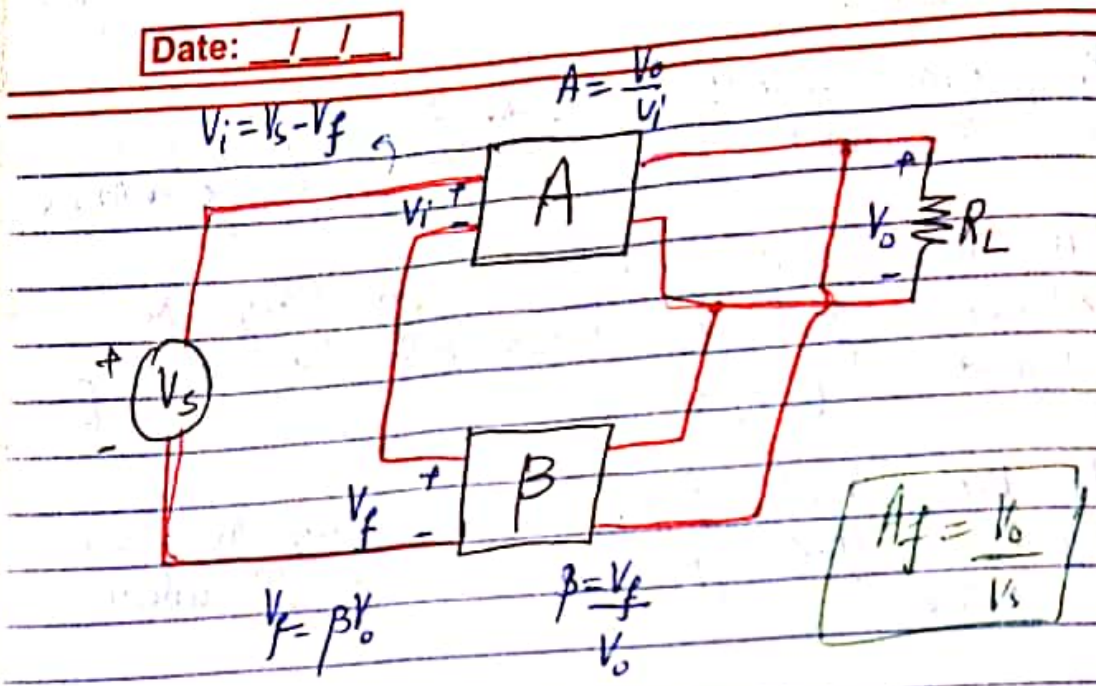
(voltage is sensed at the o/p and are substracted at the i/p).

→ i/p signal = V_s o/p signal = V_o
feedback signal = V_f i/p to amplifier = V_i

Series shunt feedback connection

Bilal Register

Date: __/__/__

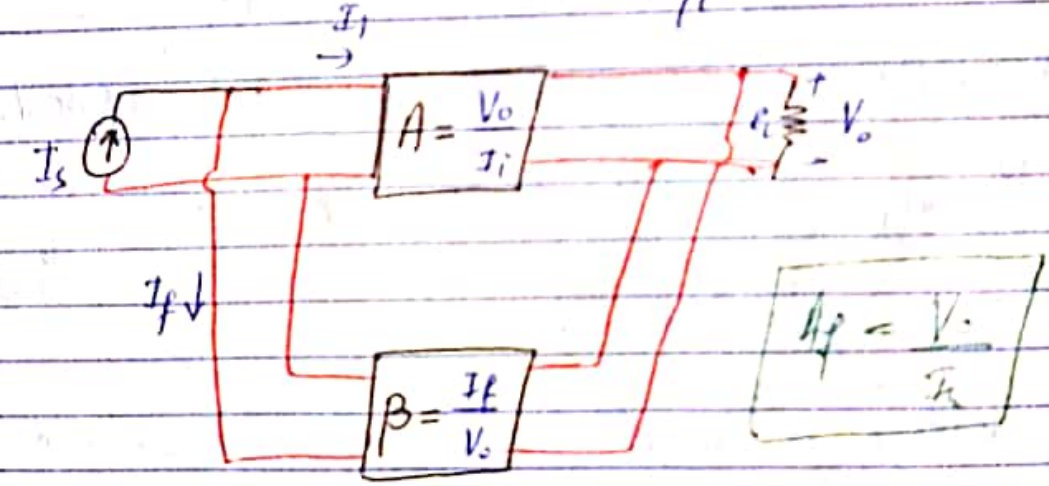


Voltage Shunt Feedback

Whenever shunt feedback → the signal save B current.

For series feedback → the i/p signal save in voltage.

↳ Here 3 currents, 1 voltage.
↳ o/p



$I_i = I_s - I_f$

↳ Also called shunt shunt feedback connection.

This is Trans resistance feedback amplifier
↳ o/p = V i/p = I
Trans Gain.

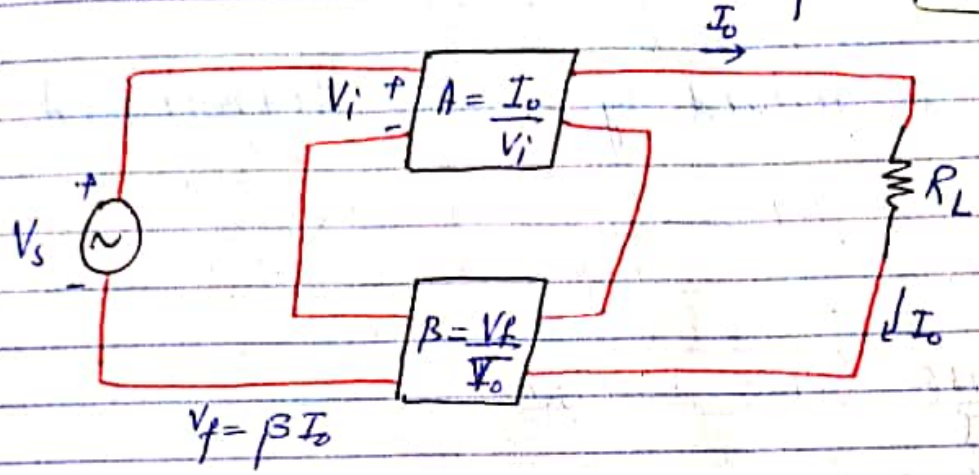
Date: / /

Current Series Feedback:

Trans ⇌ conductance feedback.
↳ I/P = V O/P = I

3 voltages, 1 current ↳ output.

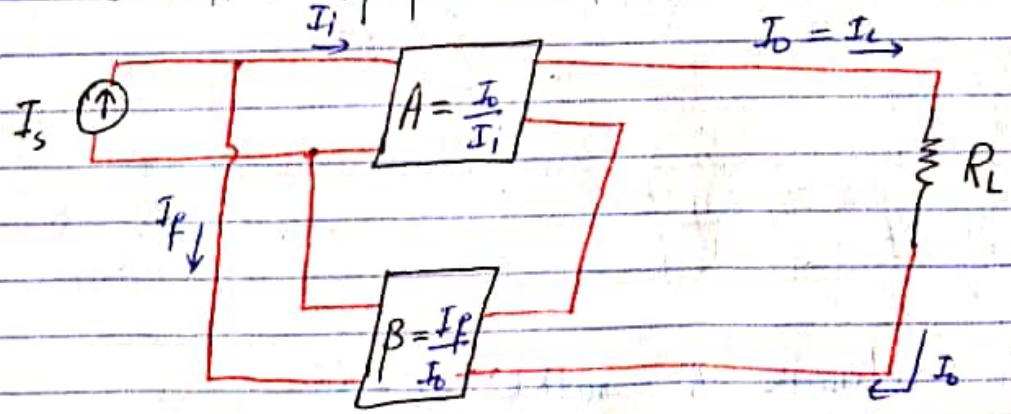
$$A_f = \frac{I_o}{V_s}$$



This is a Series series feedback connection.

Current Shunt Feedback

Current amplifier



$$I_i = I_s - I_f$$

$$A_f = \frac{I_o}{I_s}$$

This is a Shunt series feedback connection

Bilal Register

Gain with feedback, A_f.
Gain without feedback, A → gain of basic amplifier.

-ve feedback reduces the overall voltage gain.

How much?

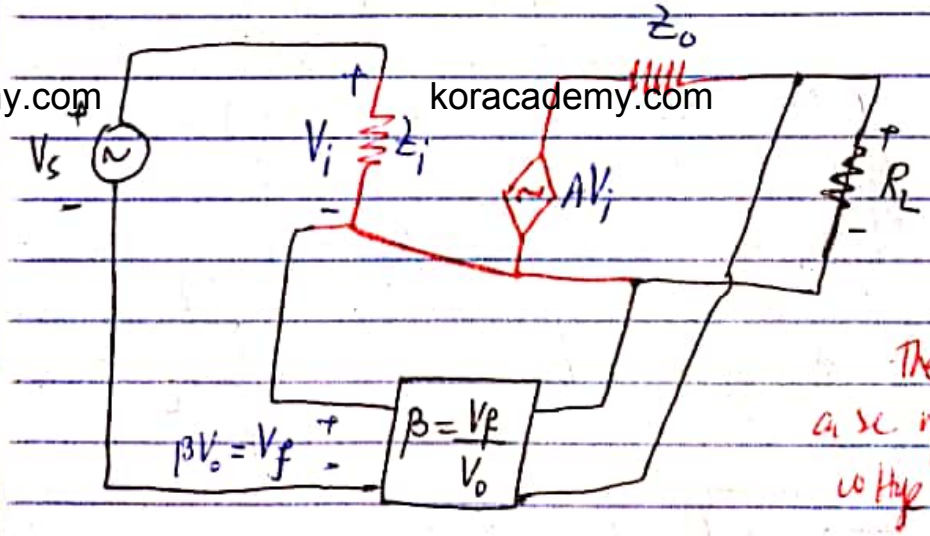
A_f is reduced by a factor $(1+\beta A)$ from A

$$A_f = \frac{A}{1+\beta A}$$

① Voltage Series Feedback.

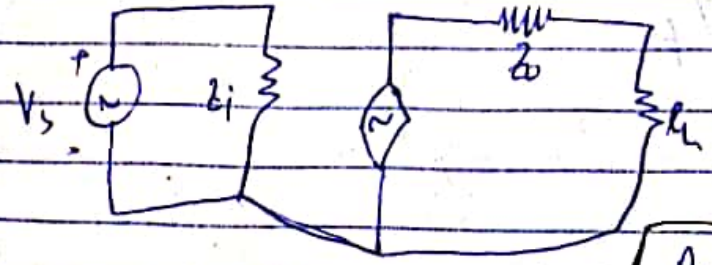
All signals are voltages.

eg of amplifier circuit.



The feedback voltage is represented by dependent voltage source.

To determine A, make $V_f = 0$



$$A = \frac{V_o}{V_i}$$

$\because V_i = V_s$

$$A = \frac{V_o}{V_i} = \frac{V_o}{V_s}$$

Date: / /

With Feedback.

$$V_i = V_s - V_f$$

$$V_o = AV_i = A(V_s - V_f)$$

$$V_f = \beta V_o$$

$$V_o = A(V_s - \beta V_o)$$

$$V_o + \beta A V_o = A V_s$$

$$V_o(1 + \beta A) = A V_s$$

$$\boxed{A_f = \frac{V_o}{V_s} = \frac{A}{1+\beta A}}$$

$A \rightarrow$ open loop gain $\quad \beta \rightarrow$ loop gain.

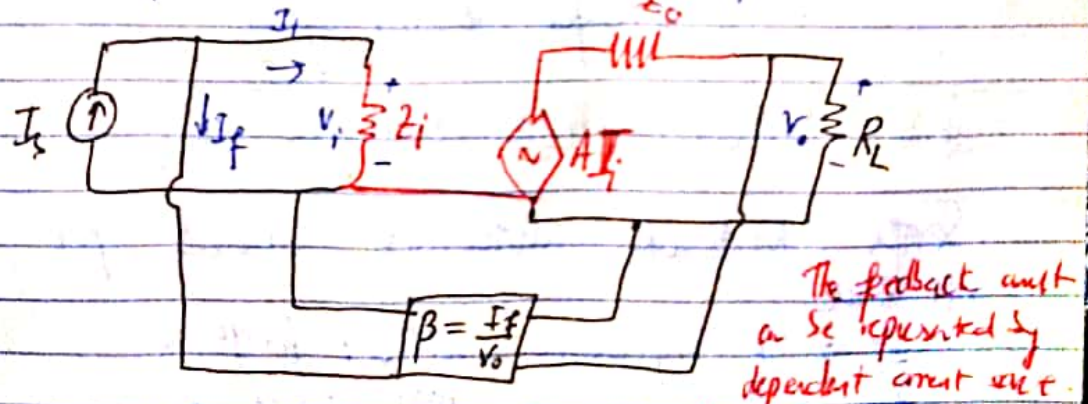
Gain has been reduced by a factor $(1+\beta A)$.

This $1+\beta A$ will also effect the input and output impedances.

(a) Voltage Shunt Feedback

All signals except the o/p signal are current signals.

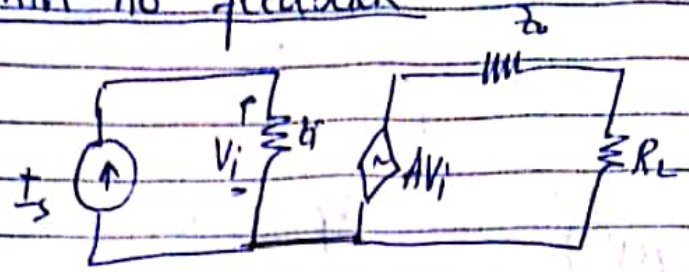
o/p is voltage $\rightarrow$ sensed in parallel



The feedback amplifier can be represented by dependent current source (voltage controlled).

Date: / /

With no feedback



$I_f = 0$

$A = \frac{V_o}{I_i}$

$I_i = I_s$

$$A = \frac{V_o}{I_i} = \frac{V_o}{I_s}$$

With Feedback

$I_i = I_s - I_f$

$$A = \frac{V_o}{I_i} = \frac{V_o}{I_s - I_f} = \frac{V_o}{I_s - \beta V_o}$$

$$A_f = \frac{V_o}{I_s} = \frac{A}{1+\beta A}$$

↳ trans resistance gain.
or trans for resistor gain.

Input Impedance With Feedback

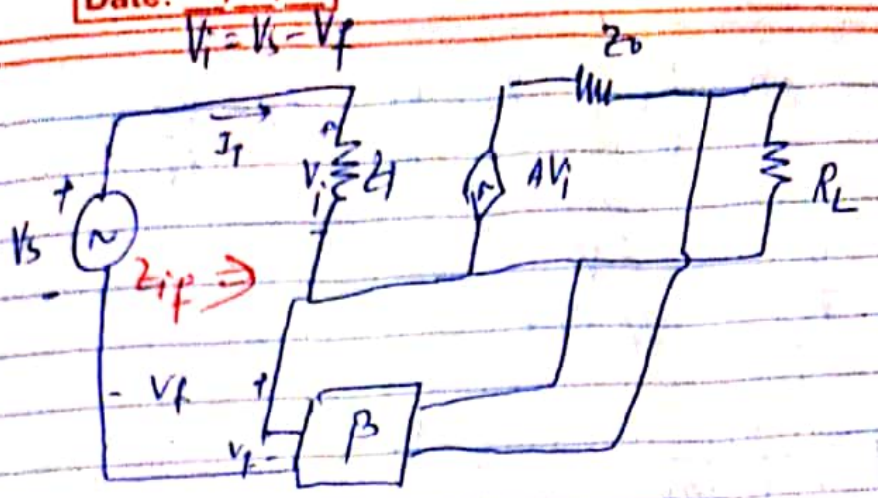
Series feedback connection increases input impedance.

Z_i → i/p impedance without feedback
Z_{if} → i/p impedance with feedback

Bilal Register

In both my voltage series and voltage shunt are there. In paper current series and current shunt is also possible.

Date: / /



$$I_i = \frac{V_i}{Z_i} = \frac{V_s - V_f}{Z_i} = \frac{V_s - \beta V_o}{Z_i}$$

$$I_i = \frac{V_s - \beta A V_i}{Z_i}$$

$$I_i Z_i = V_s - \beta A V_i$$

$$V_s = I_i Z_i + \beta A V_i$$

$$V_s = I_i Z_i + \beta A I_i Z_i$$

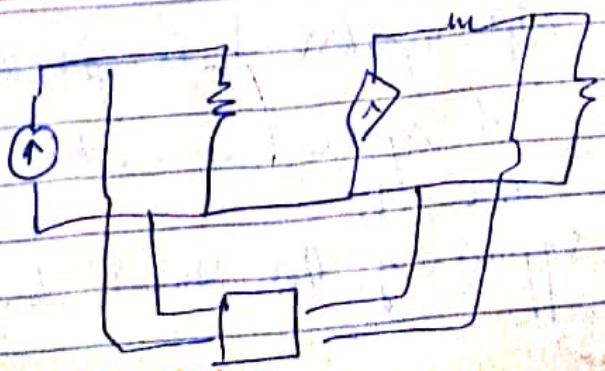
$$V_s = I_i Z_i (1 + \beta A)$$

$$\frac{V_s}{I_i} = Z_i (1 + \beta A)$$

increased.

$$\Rightarrow \boxed{Z_{if} = (1 + \beta A) Z_i}$$

② Voltage Shunt feedback



Date: / /

$A = \frac{V_o}{I_i}$ $\beta = \frac{I_f}{V_o}$ $Z_i = \frac{V_i}{I_i}$ $A_f = \frac{V_o}{I_s}$

$$Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f}$$

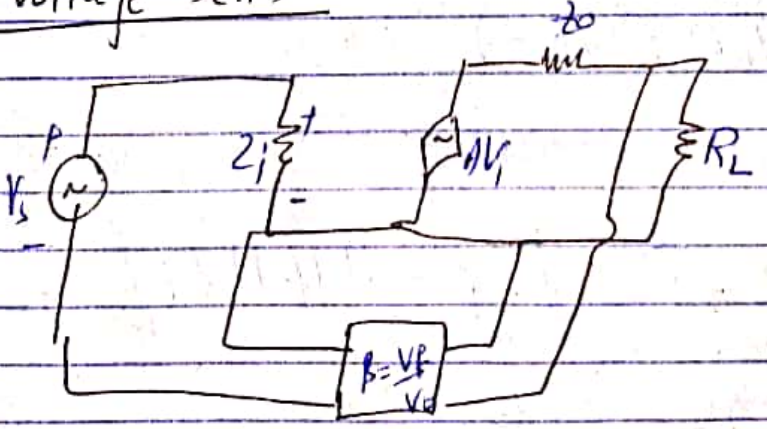
$$Z_{if} = \frac{V_i}{I_i + \beta V_o} = \frac{V_i}{I_i\left(1 + \beta \frac{V_o}{V_i}\right)}$$

$$\boxed{Z_{if} = \frac{Z_i}{1 + \beta A}}$$

Current feedback connection increases o/p impedance voltage feedback reduces o/p impedance.

Output Impedance:

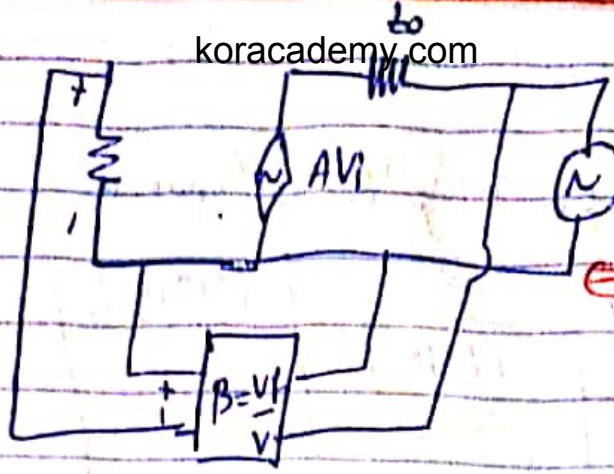
Voltage series



To determine o/p impedance V_s is grounded.

$V_s = 0$ and replace load resistance by dummy voltage source V_o.

The current supplied by this source is I.



z_{of}

$$z_{of} = \frac{V}{I}$$

$$V = I z_o + A V_i \quad , \quad V_i = -V_f$$

$$V = I z_o - A V_f \quad , \quad V_f = \beta V$$

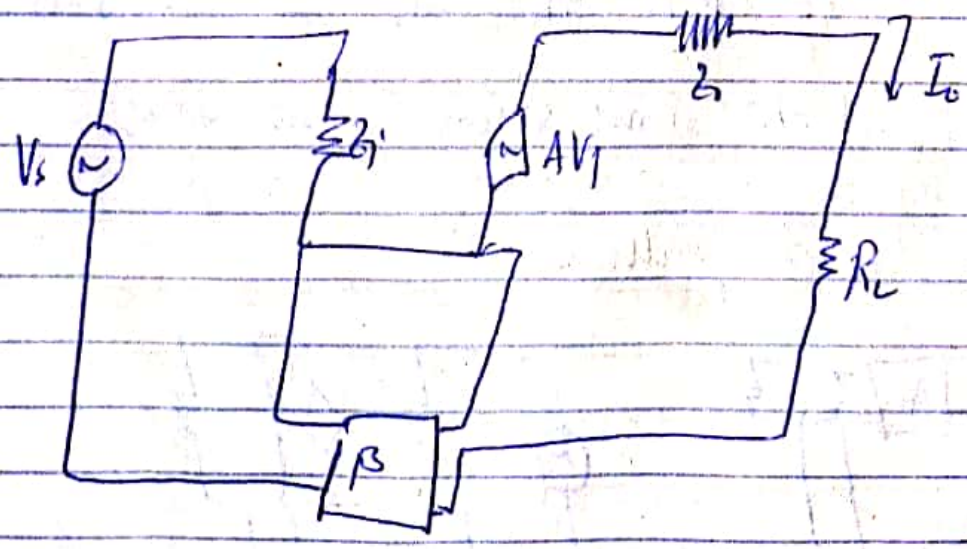
$$V = I z_o - A\beta V$$

$$V + \beta A V = I z_o$$

$$\boxed{z_{of} = \frac{V}{I} = \frac{z_o}{1+\beta A}}$$

③ Current Senes Feedback

current is sampled and voltage is mixed.



Make $V_s = 0$ Replace R_L by voltage source.

Summary

	Voltage Series	Voltage Shunt	Current Series	Current Shunt
Z_{if}	$(1+\beta A)\, Z_i$	$\frac{Z_i}{(1+\beta A)}$	$(1+\beta A)\, Z_i$	$\frac{Z_i}{(1+\beta A)}$
Z_{of}			$(1+\beta A)\, Z_o$	

Lecture 4 16/12/19.

→ Series feedback connection increases input impedance.

→ Voltage feedback decreases o/p impedance

→ Current feedback increases o/p impedance.

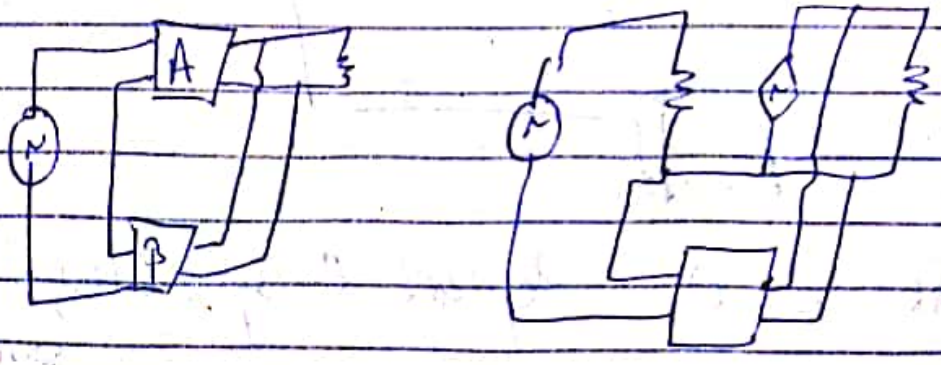
→ Voltage feedback decreases o/p impedance.

linear operation?

eg i/p is sinosidal o/p is also sinside

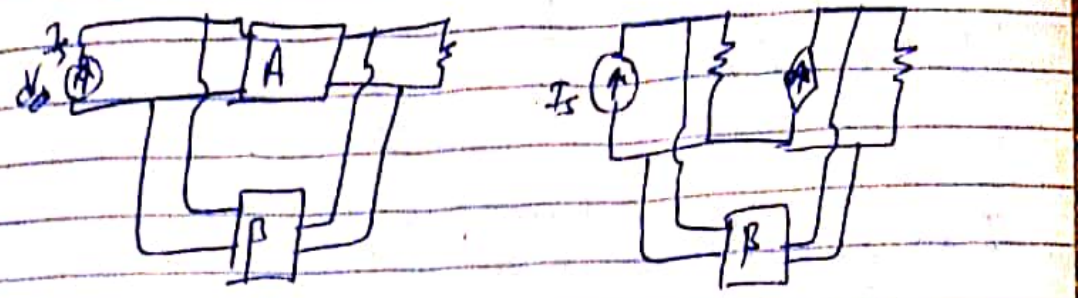
~~if i/p~~ and o/p is not similar → Non linear.

① Voltage series feedback

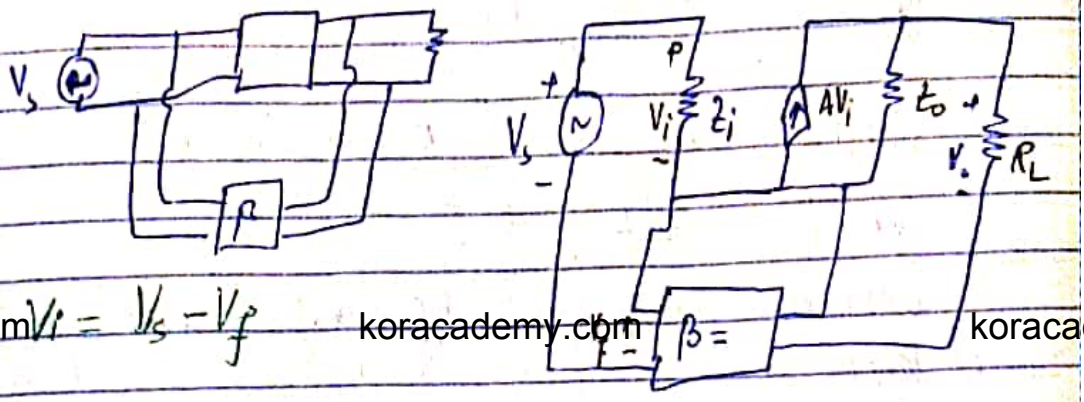


Date: / /

② Voltage shunt feedback

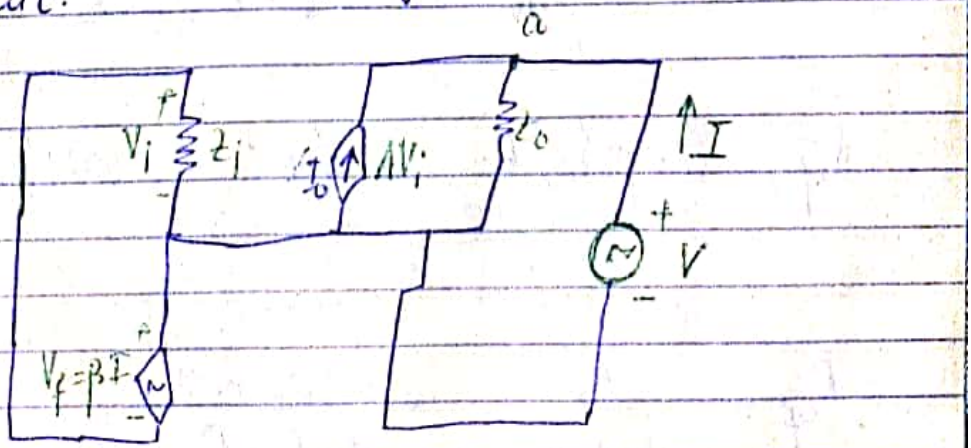


① Cunct Series feedback



$V_i = V_s - V_f$

To determine , make $V_s = 0$ and replace load resistance R_L by a dummy voltage sure V giving cunct I to the cruit.



Apply KCL at node a

$$I + I_o = \frac{V}{Z_o}$$

Bilal Register

$$A_f = \frac{A}{1+\beta A}$$

Date: / /

A > Af by a factor $1+\beta A$

$$I = \frac{V}{Z_o} - I_o = \frac{V}{Z_o} - AV_i$$

$$V_f = +V_i$$
$$V_i = +V_f$$
$$V_f = \beta I$$

$$I = \frac{V}{Z_o} + AV_f$$

$$I = \frac{V}{Z_o} + A\beta I$$

$$Z_{of} = \frac{V}{I} = (1+\beta A) Z_o$$

Ex 14.1 $A = -100$ $R_i = 10k\Omega$ $R_o = 20k\Omega$

for $\beta = -0.1$ and $\beta = -0.5$

Determine voltage gain, I/P impedance and o/p impedance.

a) For $\beta = -0.1$

$$A_{vf} = \frac{A_v}{1+\beta A_v} = \frac{-100}{1+(-0.1)(-100)} = -9.09$$

$$R_{if} = (1+\beta A_v) R_i = (1+(-0.1)(-100))(10k\Omega)$$

$$R_{of} = \frac{R_o}{1+\beta A_v} = \frac{20\,K\Omega}{1+(-0.1)(-100)} = \text{——}$$

b) similarly for $\beta = -0.5$

Bilal Register

Date: / /

Reduction in frequency distortion is the advantage for negative feedback amplifier

$$A_{vf} = \frac{A_v}{1+\beta A}$$

If $\beta A \gg 1 \Rightarrow$ $A_f \cong \frac{1}{\beta}$

→ If the feedback network is purely resistive; A_f does not depend on the frequency although A does depend on frequency.

↳ we dont want gain to vary with frequency.
↳ we want stable operation.

Frequency distortion? Variation of gain with frequency

Reduction in noise and non linear distortion

With application of negative feedback, reduces the amount of noise signal such as power supply.

Say N = noise signal without feedback
N_f = noise signal with feedback

$$N_f = \frac{N}{(1+\beta A)}$$

which means the noise signal has been reduced by a factor $1+\beta A$.

Bilal Register

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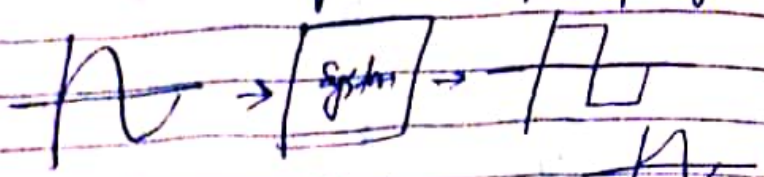
Distortion? Change in shape of signal.



sinusoidal i/p → system → non sinusoidal o/p

↳ non linear distortion.

Say D is the distortion without feedback.
and Df is the distortion after negative feedback applied.

$$\Rightarrow \boxed{D_f = \frac{D}{1+\beta A}}$$

Effect of -ve feedback on Gain and Bandwidth

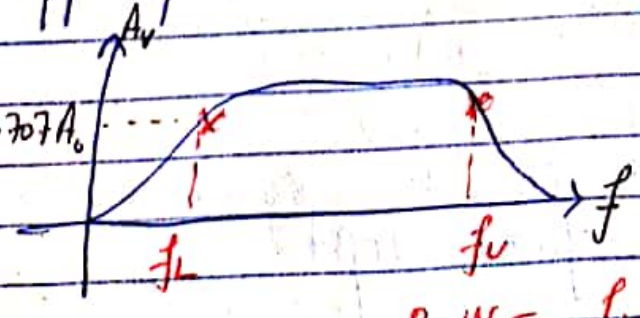
Overall Gain reduces: $A_f = \frac{A}{1+\beta A}$

If $\beta A >> 1 \Rightarrow \boxed{A_f \approx \frac{1}{\beta}}$

For Bandwidth?

Difference b/w upper and lower cut off frequencies.

x → Half power points



$B.W = f_U - f_L$

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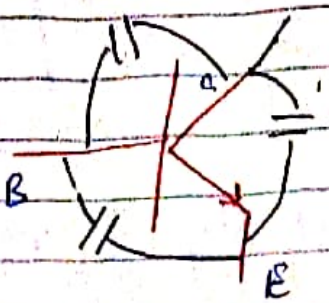
→ Normally open loop gain reduces as frequency increases due to active device and capacitances.



$X_C = \frac{1}{2\pi f C}$

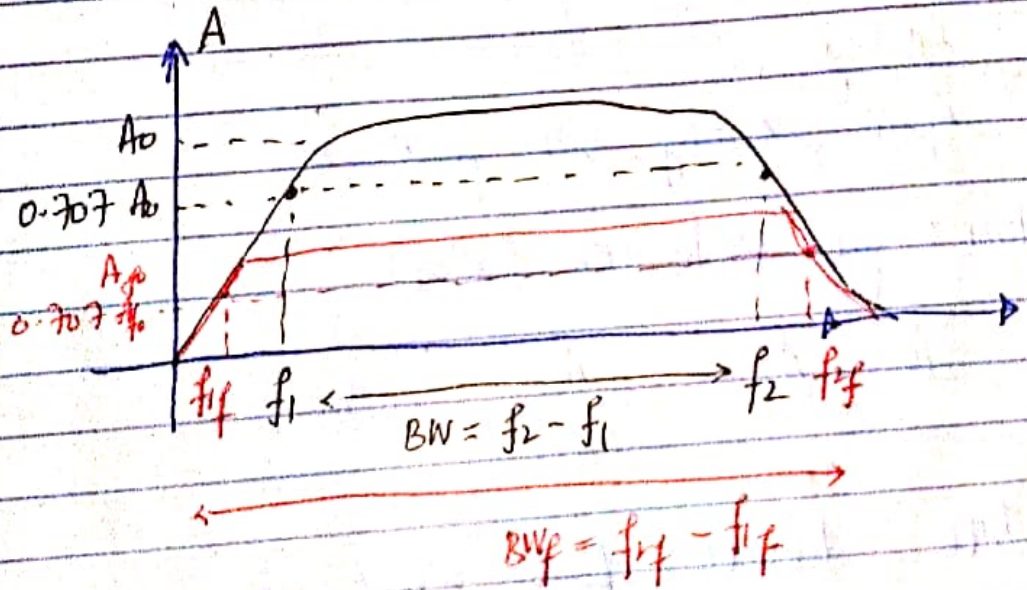
At high frequency → these capacitors → short circuit behaviour

↳ very small amount of signal appears at the base of transistor

↳ Hence o/p is reduced.

These capacitors are called stray capacitors.

B.W without feedback,



→ Overall gain has been reduced.

→ Device is operating linearly over a large range of frequencies.

Date: / /

The gain bandwidth product with and without feedback is same.

$$A \times BW = A_f \times BW_f$$

As A_f is decreased and BW_f is increased by $1+\beta A$.

f_2 is increased by factor $1+\beta A$
f_1 is decreased by factor $1+\beta A$.

Normally $f_2 >> f_1$

So the upper cut off frequency becomes the bandwidth.

Stability

Gain stability with feedback.

How is gain stable with feedback?

As $$A_f = \frac{A}{1+\beta A} \rightarrow (1)$$

Take derivative of (1) w.r.t A

As $$\frac{d}{dx}\left(\frac{u}{v}\right) = \frac{v\,du - u\,dv}{v^2}$$

$$\frac{dA_f}{dA} = \frac{(1+\beta A) - A(\beta)}{(1+\beta A)^2} \rightarrow$$

Date: / /

If voltage gain has been reduced now to increase it to a desired level, we use cascading.

$$\rightarrow \frac{1+\beta A-\beta A}{(1+\beta A)^2} = \frac{1}{(1+\beta A)^2}$$

divide and multiply by A

$$= \frac{A}{A(1+\beta A)^2} = \frac{A}{A(1+\beta A)(1+\beta A)}$$

$$= \frac{A_f}{A(1+\beta A)}$$

$$\boxed{\frac{dA_f}{dA} = \frac{A_f}{A(1+\beta A)}}$$

$$\left|\frac{dA_f}{A_f}\right| = \left|\frac{1}{1+\beta A}\right| \left|\frac{dA}{A}\right|$$

If $\beta A \gg 1$

$$\boxed{\frac{dA_f}{A_f} = \left|\frac{1}{\beta A}\right| \left|\frac{dA}{A}\right|}$$

$\left|\frac{dA_f}{A_f}\right|$ is the magnitude of relative / fractional change in gain with feedback and is reduced by factor $\left|\frac{1}{\beta A}\right|$ compared to relative change in magnitude $\left|\frac{dA}{A}\right|$ without feedback.

Bilal Register

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Example Gain, $A = -1000$
Feedback factor, $\beta = -0.1$ has a gain change of 20% due to temperature. Calculate the change in gain of the feedback amplifier.

$$\text{Gain change} = \left|\frac{dA}{A}\right| = 20\% = 0.2$$

$$\text{As } \frac{dA_f}{A} \simeq \left|\frac{1}{\beta A}\right| \left|\frac{dA}{A}\right|$$

$$= \left[\frac{1}{-0.1 \times -1000} \times 20\%\right] = 0.2\%$$

So the improvement is 100%.

$$\text{As } \frac{20\%}{0.2\%} = 100$$

$$A_f = \frac{A}{1+\beta A} = \frac{-1000}{1+100} = \frac{-1000}{101}$$

$$\Rightarrow |A_f| \simeq 10$$

Gain has been reduced 10 times but stability has increased 100 times.
↳ due to feedback.

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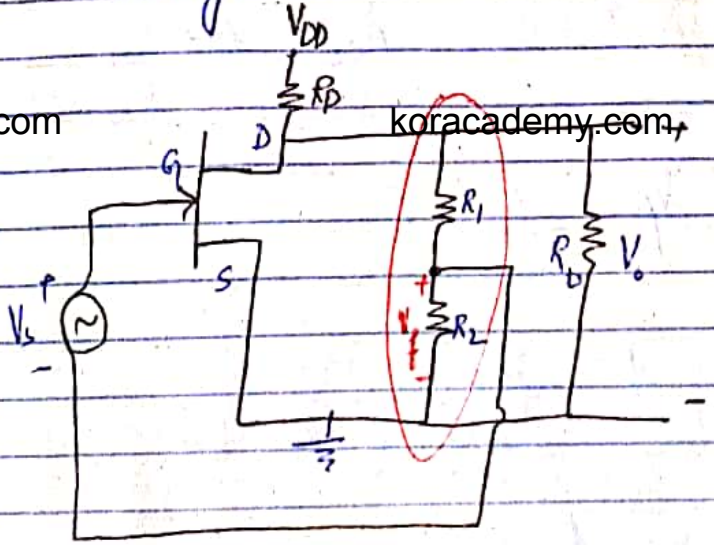
Application of Topologies.

→ We have sampling at the o/p of the feedback amplifier and we have mixing at its i/p.

→ If the o/p and feedback both are at the same terminal Then it means voltage sampling otherwise current sampling.

→ On the i/p side if the source and the feedback both are at the same terminal then it is called shunt mixing. otherwise series mixing.



Voltage divider rule

$$V_f = \frac{R_2}{R_1+R_2} V_o$$

$$A = \frac{V_o}{V_i} = -g_m R_L$$

Voltage series feedback connection. $R_L = R_D \| R_o \| (R_1+R_2)$

↳ series mixing.

source and feedback are not at the same point ∴ in series.

$$\beta = \frac{V_f}{V_o} = \frac{R_L}{R_1+R_2} \quad , \quad A_f = \frac{A}{1+\beta A}$$

$$A_f = \frac{1}{\beta} \qquad \beta A >> 1$$

Bilal Register

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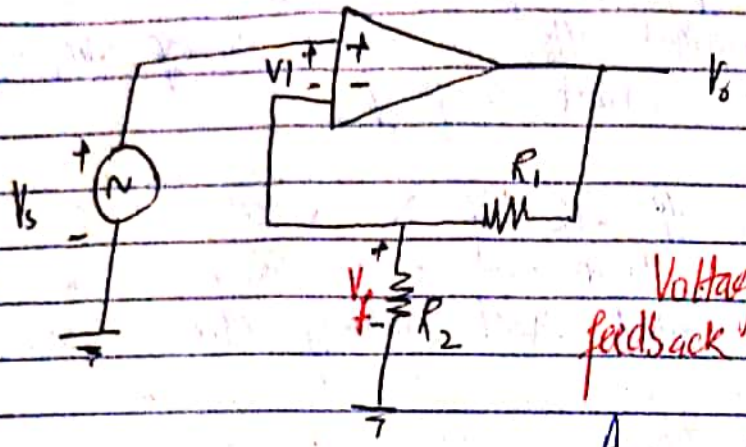
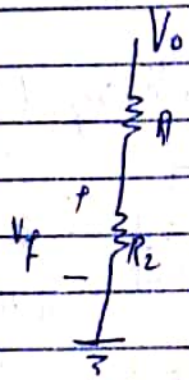
$$A_f = \frac{R_1+R_2}{R_2} = -\left(1+\frac{R_1}{R_2}\right)$$

due to common source amplifier.



Voltage series feedback connection.

$$A_{CL} = 1 + \frac{R_1}{R_2}$$



$$V_f = \frac{R_2}{R_1+R_2} V_o$$

$$\beta = \frac{V_f}{V_o} = \frac{R_2}{R_1+R_2}$$

Open loop gain, $A = \infty$

$$A_f \cong \frac{1}{\beta A} \quad \text{if } \beta A >> 1$$

$$A_f = \frac{R_1+R_2}{R_2} = 1 + \frac{R_1}{R_2}$$

Practically range of $A = 10^5 - 10^6$

Bilal Register

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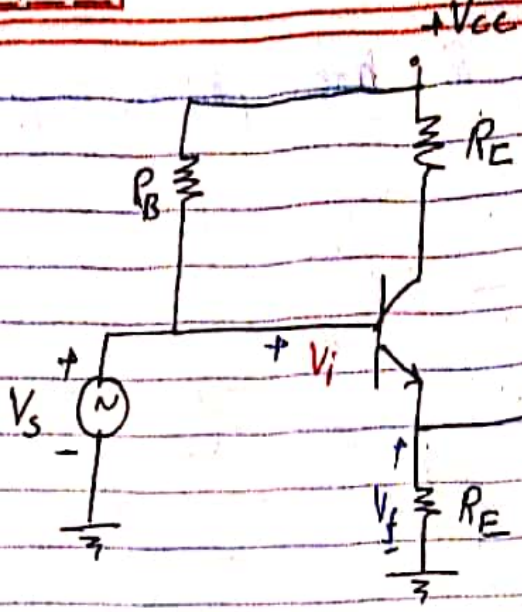

Common collector
OR
Emitter follower configuration.

I/P is applied at base.
O/P is taken at emitter.

O/P across R_E. Feedback also at R_E.
↳ Here $V_s = V_i$ $V_o = V_f$

source and feedback are not at same terminal.
↳ voltage series feedback connection.

$$A = \frac{V_o}{V_i} = \frac{V_o}{V_s} = \frac{h_{fe} I_b R_E}{V_s}$$

$$I_c = h_{fe} I_b \approx I_e \qquad I_b = \frac{V_s}{h_{ie}}$$

$$\beta = \frac{V_f}{V_o} = 1$$

$$A = \frac{h_{fe} R_E \left(\frac{V_s}{h_{Ie}}\right)}{V_s} = \frac{h_{fe} R_E}{h_{ie}}$$

$$A_f = \frac{V_o}{V_s} = \frac{A}{1+\beta A} = \frac{h_{fe} R_E}{h_{ie} + h_{fe} R_E}$$

If $h_{fe} R_E \gg h_{ie} \Rightarrow A_f \approx 1$

Bilal Register

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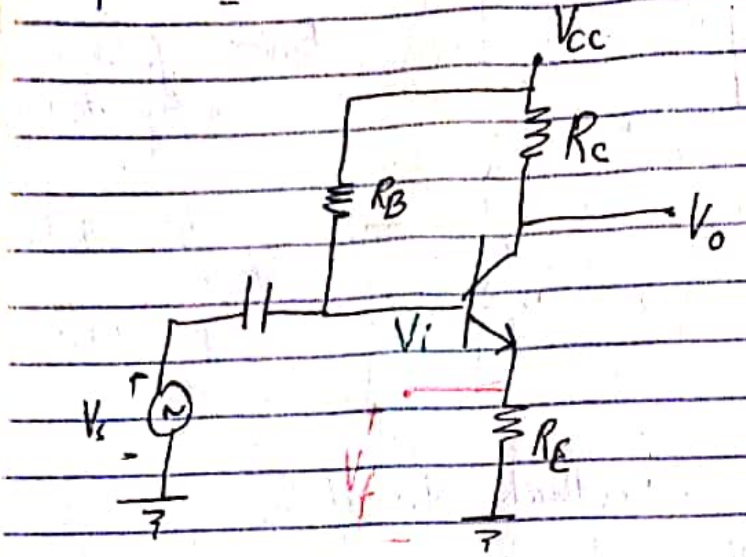
The resistor R_E here provides negative feedback.



Feedback and o/p are not at the same terminal
↳ Current sampling

i/p side → same and feedback are not at same terminal → series:

Current Series feedback connection.

→ To remove feedback from emit either directly ground the emitter terminal or (normally) places a bypass capacitor across R_E.

→ o/p is current, i/p is voltage.

$$A = \frac{I_o}{V_i} = \frac{h_{fe} I_b}{I_b h_{ie}} \qquad A = -\left(\frac{h_{fe}}{h_{ie}}\right)$$

trans conductance gain

h_{fe} → current gain h_{ie} → ohms

Bilal Register

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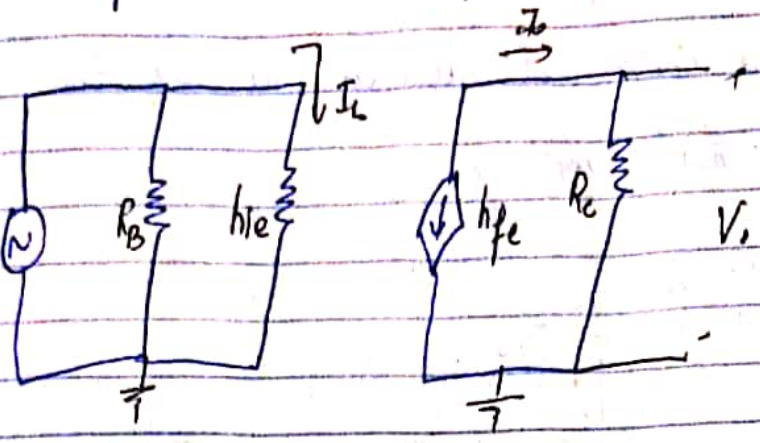
$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_E}{I_o} = -R_E$$

The equivalent circuit for the shunt circuit is as;



$$z_i = R_B \,||\, h_{ie} \qquad R_o = R_c$$

$$A_f = \frac{A}{1+\beta A} = \frac{I_o}{V_s}$$ transconductance gain.

Put value of A and β in this eq.

$$A_f = \frac{-h_{fe}}{h_{ie} + h_{fe} R_E}$$

$$z_{if} = z_i (1+\beta A)$$

$$z_{of} = z_o (1+\beta A)$$

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_c}{V_s} = A_f R_c$$

$$A_{vf} = \frac{-h_{fe} R_c}{h_{ie} + h_{fe} R_E}$$

Bilal Register

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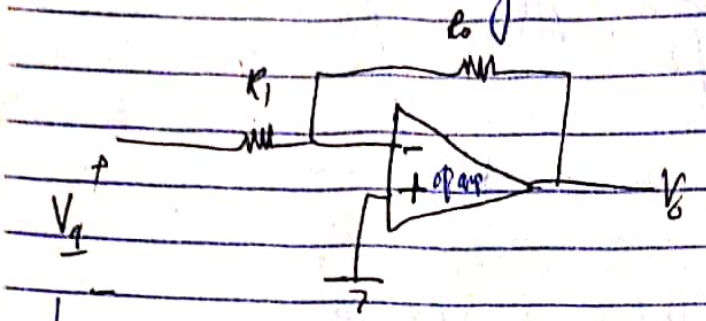
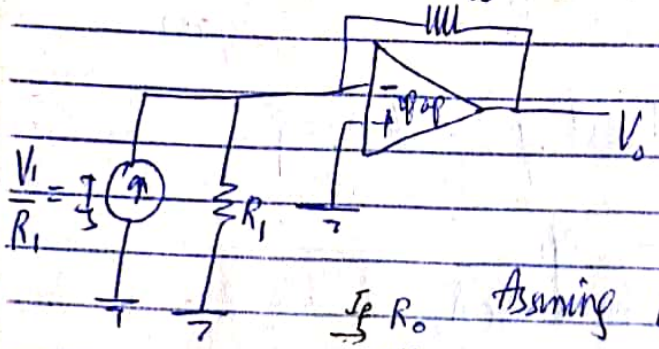
Voltage Shunt feedback Connection

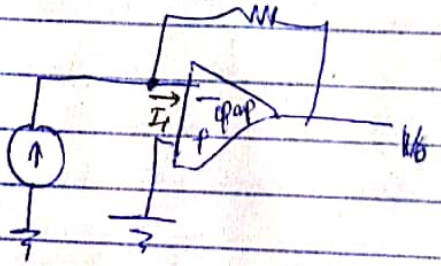
o/p side → feedback ckt o/p at same terminal
↳ voltage sampling

I/p side → source and feedback at same terminal
↳ shunt mixing.



↳ Replacing V_i by ament source.





Assuming R_i to be very large

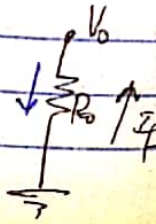
$$A = \frac{V_o}{I_i}$$

Ideally $I_i = 0$

$\Rightarrow A = \infty$

$$\beta = \frac{I_f}{V_o}$$

$$I_f = \frac{-V_o}{R_o}$$



Bilal Register

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$$\beta = \frac{-1}{R_0}$$

$$A_f = \frac{A}{1+\beta A} \approx \frac{1}{\beta} = -R_0$$

$$I_s = I_f + I_i \quad (I_i \to 0)$$

$$I_s = I_f$$

$$A_f = \frac{V_0}{I_s} = \frac{V_0}{I_f} = \frac{A}{1+\beta A}$$

↳ transfer resistor gain.

But we are interested in voltage gain.

$$A_{vf} = \frac{V_0}{V_i} \times \frac{I_s}{I_s} = \frac{V_0}{I_s} \times \frac{I_s}{V_i}$$

$\frac{V_0}{I_s} \downarrow A_f$

$$\boxed{A_{vf} = \frac{-R_0}{R_i}}$$

Lecture 5 — 23/12/19

|Gain x Bandwidth| = |Gain x Bandwidth|

(Gain: no dimension; ↳ unit B Hertz.)

without feedback — with feedback

Gain ↑ B.W ↓ Gain ↓ BW ↑

↳ frequency response improves.

Constant Gain for a large range of frequency stable.

Bilal Register

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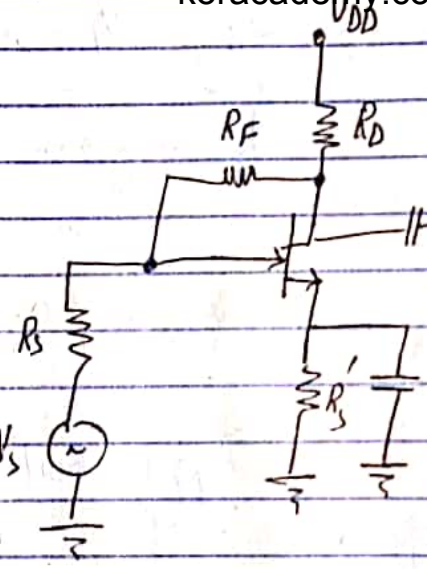
→ Sampling is performed at the o/p side
→ Mixing at the i/p terminal.

~~If source~~ $1+\beta A$ is called Gain Desensitivity factor.

To analyze the circuit;
(i) First determine A or β.
↳ By removing feedback component from the circuit.
β is determined in the presence of feedback
(ii) Finally determine the gain with feedback.

$$A_f = \frac{A}{1+\beta A}$$



This is voltage shunt feedback connection

This is trans resistance amplifier. i/p is voltage and i/p is current.

Convert the voltage source to current source and redraw the circuit.

In voltage shunt o/p is voltage and other three signals are currents.

Bilal Register

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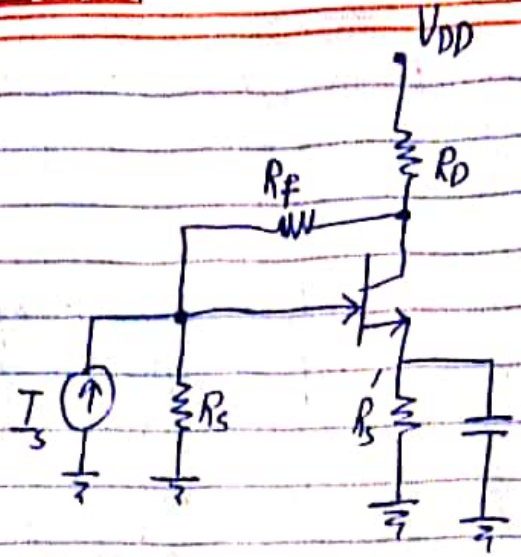
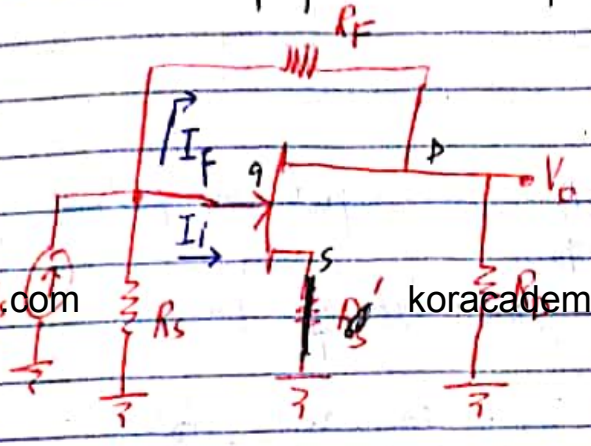


The simplified AC equivalent circuit is as;



Mathematical derivation yourself.

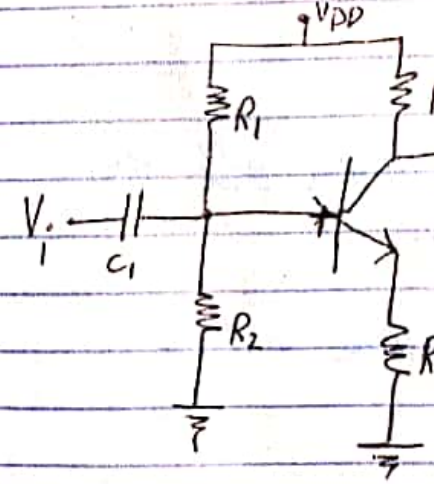
$(A = -g_m R_D R_S)$

$\left(\beta = I_o/V_o = -1/R_f\right.$

$\left. A_f = \frac{V_o}{I_s} = \frac{A}{1+\beta A}\right)$

Stability

How to determine if amplifier is stable or not?



RE provides feedback.

Sampling = current.

feedback and i/p not at same terminal = series.

So this is a current series feedback amplifier.

Bilal Register

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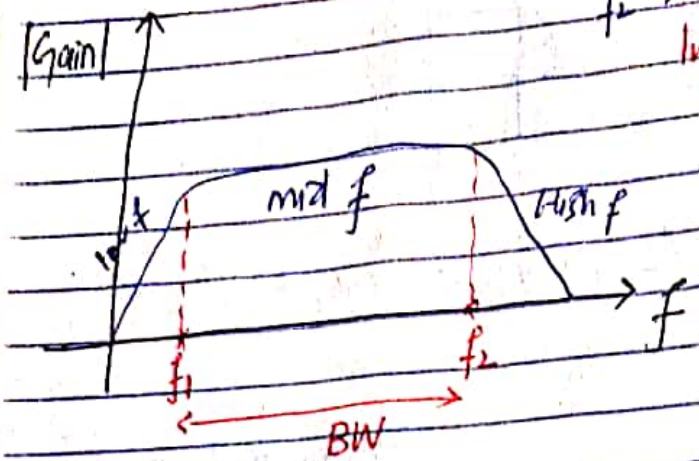
We are interested in voltage amplification of the device.

Ex 14.6.



f_1 → lower cut off
f_2 → upper cut off
In mid frequency region, we had maximum gain.

In negative feedback, i/p signal and feedback signal oppose each other.
↳ They are 180° out of phase.

The Gain is stable in mid frequency range.
↳ -ve feedback occurs.

Phase changes with frequency.

↳ $f \uparrow \Rightarrow G \downarrow$

↳ B/w o/p and i/p signal
↳ Rather than opposing each other, they will add into each other.
↳ o/p will increase
↳ System will become instable.

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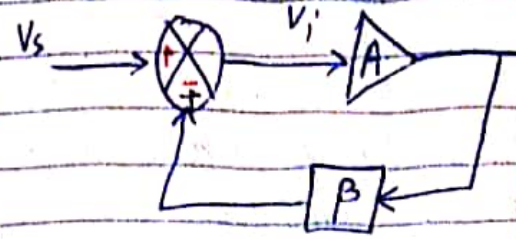
-ve feedback $V_i = V_s - V_f$



At phase changes;

+ve feedback

$V_i = V_s + V_f$

Here $V_i > V_s$ by amount of V_f.

↳ occurs when frequency changes → Except the mid frequency range.

In oscillator we do not require source signal.

We require an amplifier that works properly with a stable gain at all frequencies.

Nyquiest Criteria

to judge stability of amplifier.

Stability of feedback amplifier is a function of frequency.

Two factors are responsible to tell about stability of the amplifier circuit.

(1) Loop gain ie βA product.
(2) Phase shift b/w i/p and o/p.

{Gain vs Frequency
Phase vs Frequency} Bode plots.

↳ If they are drawn on the same plane (plot), then they are called nyquist plot.

The Nyquiest diagram shows both gain and

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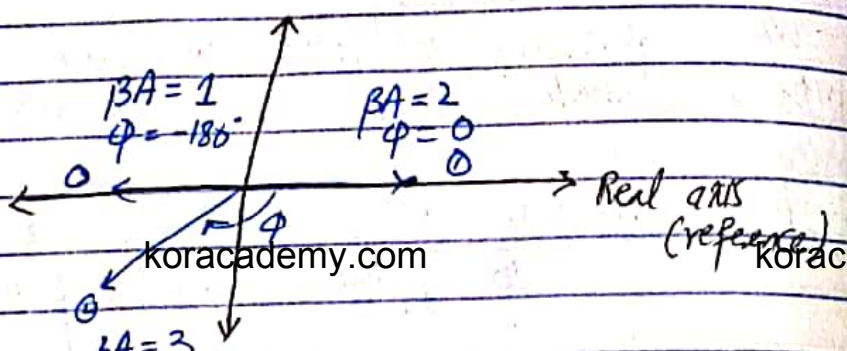
In complex plane

phase together on a same plot as a function of frequency.

The Nyquist plot will tell us whether the system is stable or unstable.

The product βA is represented by a vector.

Here in place of direction, we will use the phase (which actually shows the direction)

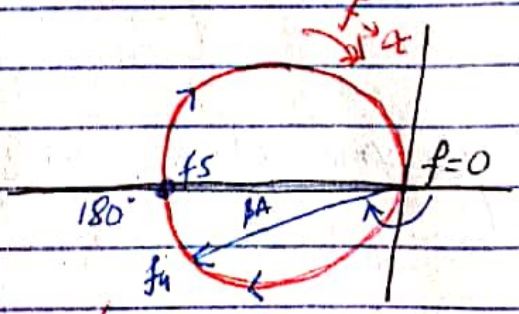


As $z = |z| \angle z$

$\beta A = |\beta A| \angle \beta A$

The points represent both magnitude and phase shift.

If these gain and phases;
4 are plotted with an increasing frequency, they represent a nyquist plot



Gain ↑ as f ↑
After some point-
as f ↑ Gain ↓

Nyquist plot

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At origin gain is zero at frequency also equal to zero for RC type coupling

At increasing frequency, points f_1, f_2, f_3 and the phase shift increase as does the magnitude of βA.

At a representative frequency f_4, the value of βA is the vector length from origin to f_4 and phase shift ϕ.

At f_s, the phase shift is 180°,
At higher frequencies the gain is shown to decrease back to zero.

$\beta A = -1 \quad |\beta A| = 1$ at $\phi = 180°$

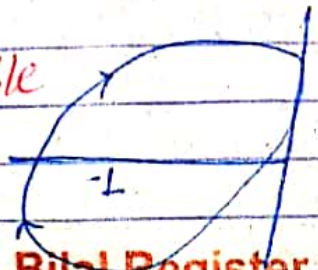
The amplifier is unstable if the nyquist curve encloses / encircles the -1 point; otherwise it is stable.

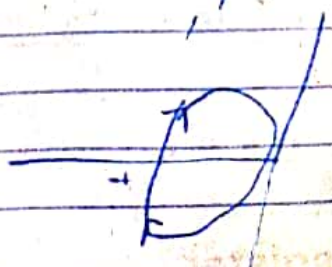
As $A_f = \frac{A}{1+\beta A}$ Normally $A_f < A$

If we put $\beta A = -1$

$\Rightarrow A_f = \infty$ and the system becomes unstable

↳ And the same feedback amplifier starts oscillation rather than amplification





At $\beta A = -1$ $\phi = 180°$

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For phase;

say an RC circuit

$$z = R - jX_c$$

$$\phi = -\tan^{-1}\left(\frac{-X_c}{R}\right)$$

Two Quantities
Gain Margin And Phase Margin

According to Nyquist criteria, feedback amplifier is stable if the loop gain is less than 1 at an angle of 180°.

magnitude of

We can additionally add some margins of stability to indicate how close to instability the amplifier ckt is.

$\beta A = 0.95$ $\beta A = 0.75$

↳ more stable.

Both are stable but $\beta A = 0.75$ is more stable, even if both are at an angle of 180°.

Gain margin is defined as negative of the value of βA in decibels at the frequency at which phase angle is 180°

0 dB corresponds to $\beta A = 1$

(Value of βA means βA mod ie absolute value)

→

Any negative value is stable.

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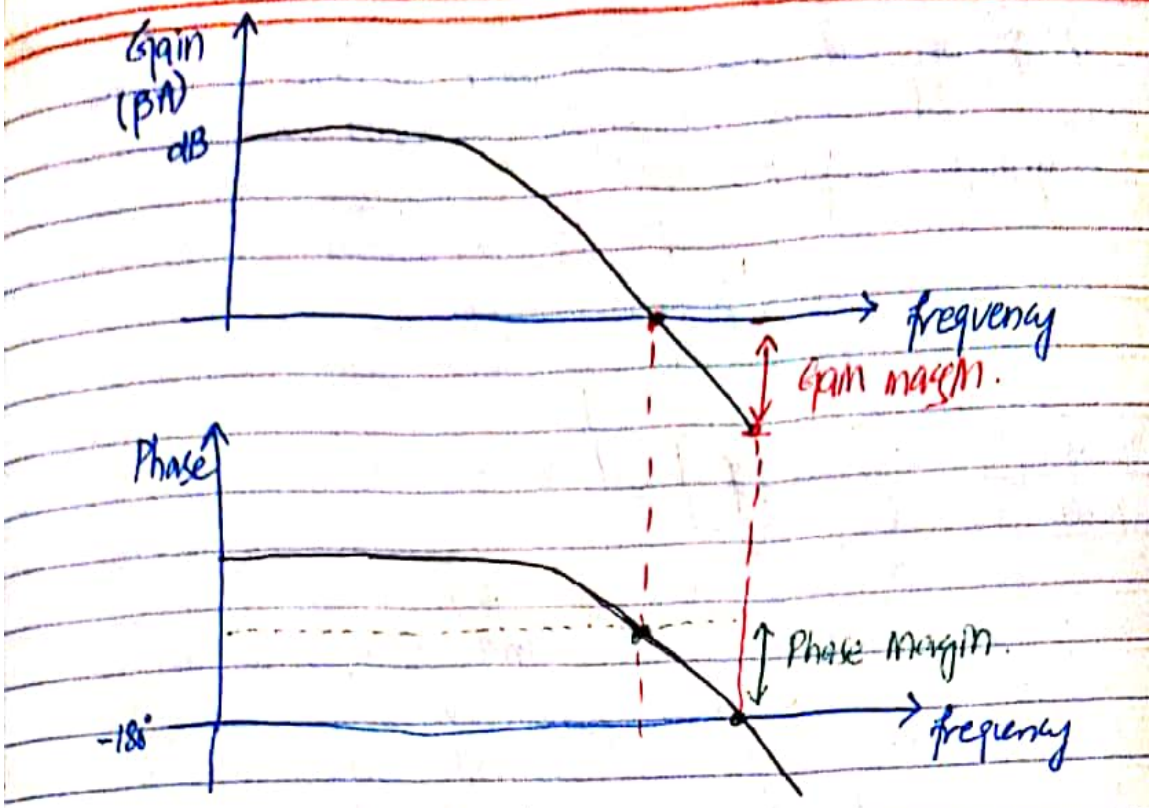

Phase Margin is defined as the angle of 180° minus the magnitude of the angle at which the value βA mod is unity or 0dB.

Oscillator Operation:

Feedback

+ve feedback (Oscillator)

-ve feedback (Amplifier)

$\beta A = -1 \rightarrow$ Circuit is unstable

With +ve feedback, the closed loop gain becomes greater than 1 and the circuit starts oscillation.

Oscillator require two components;

(i) Amplifier part

(ii) Feedback network (frequency selective network).

Bilal Register

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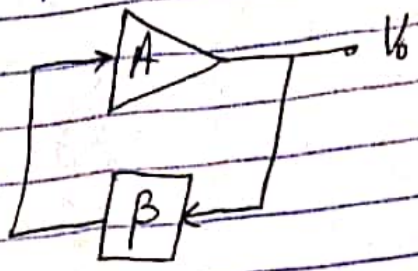
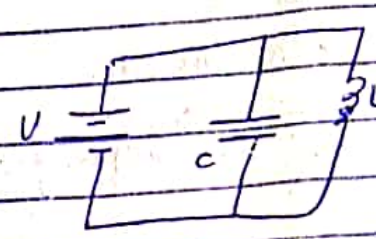
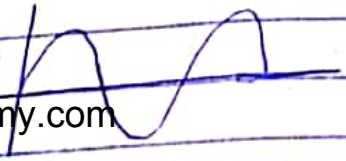
We can say that oscillator converts DC to AC
↳ B/c we apply DC and we get a varying output.



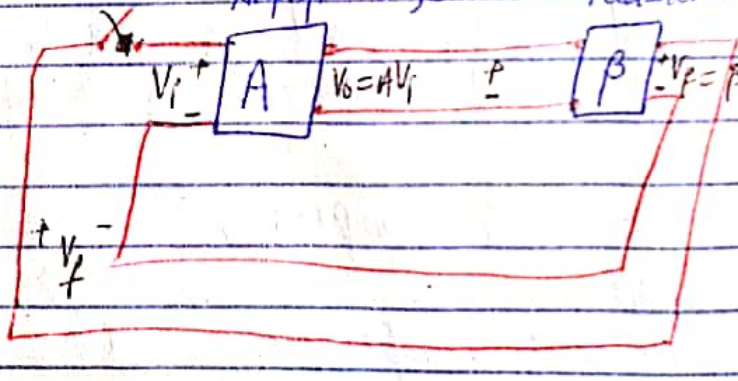


charge C by V and then remove V_o.
C will discharge through L.
Now L is charged which discharges through C. In this process it repeats.



→ For sustained oscillation we require amplifier circuit.

Oscillator provides a varying o/p signal.
↳ classified into two types.
(i) Sinusoidal oscillators
(ii) Non sinusoidal / Relaxation oscillators.



Bilal Register

Date: / /

When switch is open; say V_i is a fictitious voltage connected.

↳ No oscillation occurs.

The feedback voltage is such that if we remove the V_i, the V_f is still capable to operate the amplifier and feedback stage.

(If the circuit of amplifier and feedback provide βA of correct magnitude (ie 1) and phase then V_f can be made equal to V_i.)

Then close the switch, remove V_i and the circuit will continue to operate since the feedback signal is sufficient to drive the amplifier and feedback circuits. resulting in a proper input voltage to sustain

Fictitious voltage is basically thermal noise in the circuit.

↓

have multiple frequencies.

Feedback is frequency selector.

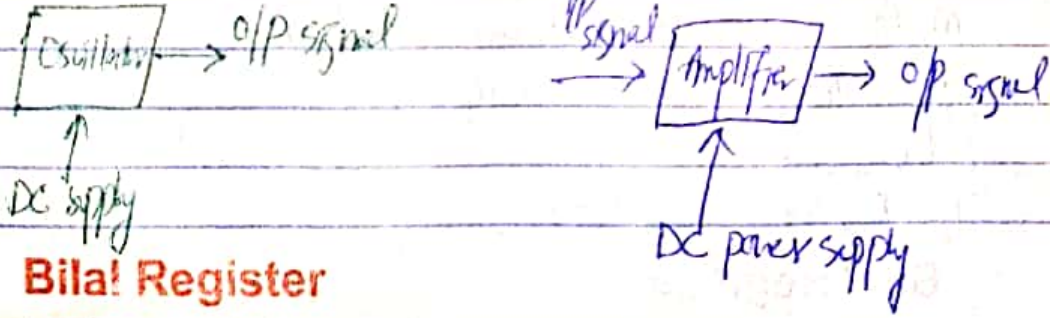
{For sustained oscillation; $\beta A = 1$

magnitude = 1 Overall phase shift = 0° or 360°

↳ Barkhausen criteria

Sustained → constant amplitude oscillation.

Oscillator does not require an applied signal.



Bilal Register

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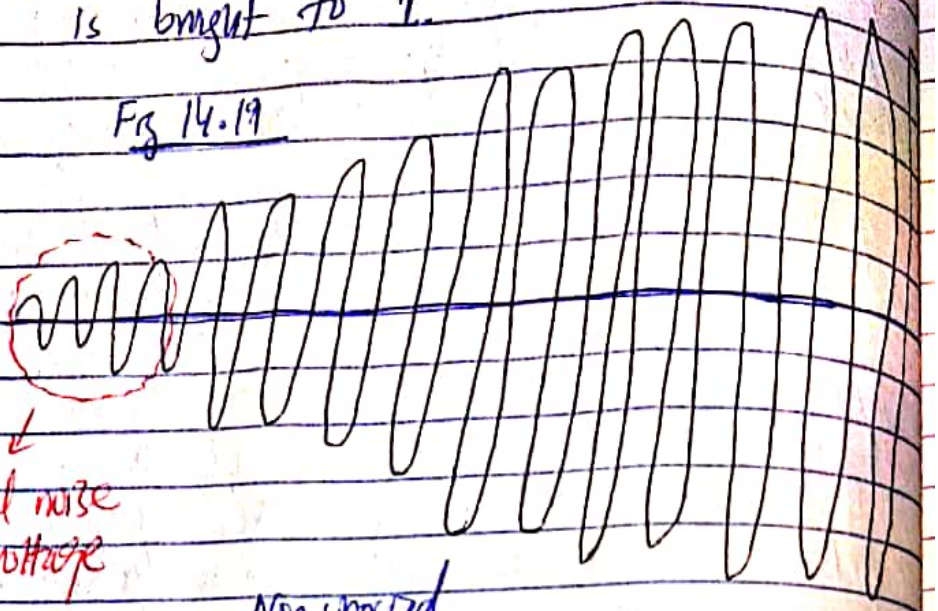
In practice, to start oscillation, initially, βA is kept greater than 1.
Once we have sustained oscillation, βA is brought to 1.

Fig 14.19



Oscillator is an amplifier with positive feedback.

$\beta A = -1$ $\quad A_f = \frac{A}{1+\beta A} \Rightarrow A_f = \infty$ ↓ unstable

oscillation ←

We start with sinusoidal oscillators.

Amplifier is the gain element.
- ↳ Transistor → BJT
  - ↳ FET
- ↳ Op Amp

Sinusoidal oscillators are categorized as;
(i) RC ~~Phase shift~~ oscillator.
(ii) LC oscillator
(iii) Crystal oscillators.

Bilal Register

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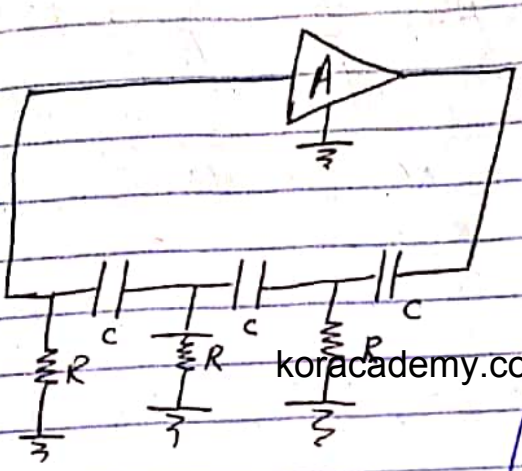
RC oscillator → Phase shift oscillator
→ Wein Bridge oscillator.

Phase Shift Oscillator

It is a low frequency oscillator.

The idealized phase shift oscillator is as,



180° phase shift is provided by feedback circuit and 180° by amplifier network.

So the overall phase shift is 0° or 360°.

Three RC sections.

The individual phase shift provided by each section may or may not be 60° each.

↳ b/c of loading effect.

Each RC section is loaded by following section.

To avoid loading phenomena, we can connect an emitter follower circuit.

General formula for frequency of oscillation is

$$f_r = \frac{1}{2\pi RC\sqrt{2n}}$$

n → no. of RC stages in the circuit.

Bilal Register

if $\beta A > 1$ then oscillations are developed with increasing amplitude.

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Feedback network provides two functions;
(i) Attenuation (β)
(ii) Desired phase shift

For RC phase shift oscillator $\beta = \frac{1}{29}$

At $\beta A = 1 \Rightarrow A = 29$

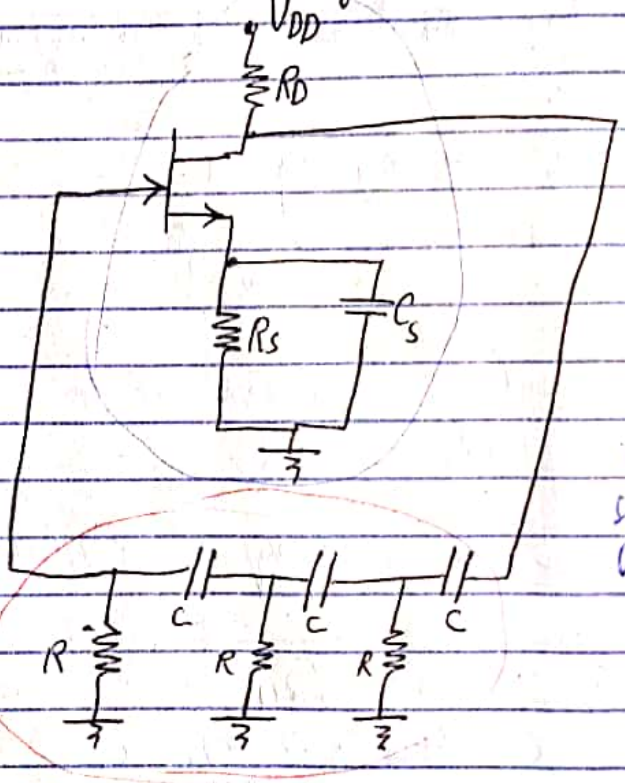
For self starting of oscillator;

$\beta A > 1$; $A > \frac{1}{\beta}$ or $A > 29$

Ideally individual RC section must provide $60°$ here as $n = 3$.

Overall phase shift provided by feedback network must be $180°$.

Practical Circuit of Phase shift Oscillator



Amplifier
Feedback

Self biased common source amplifier with Rs bypassed by capacitor Cs.

Bilal Register

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For amplifier g_m and r_d are the quantities of interest.

$$|A| = g_m R_L \qquad R_L = r_d \,||\, R_D$$

Approximation.

→ Input impedance is very high (ideally infinite)

These are low frequency oscillators.

As frequency increases, the stray capacitances become active and create a problem.

→ o/p impedance of amplifier stage is R_L.

R_L should be smaller than the impedance looking into the feedback network to avoid loading effect.

Lecture 6 30/12/19

Nyquist Stability Criteria.

Stability ? By changing frequency, there should be no change in gain of the amplifier.

Nyquist curve should not ~~map~~ include -1 point otherwise it is unstable.

$$A_f = \frac{A}{1+\beta A}$$

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If $\beta A = -1$ $A_f = \infty$

↳ Now this will not work as ~~oscillator~~ amplifier; it will produce oscillations at the o/p

Gain Margin? Phase margin?

0.75 and 0.95 gain values.

↳ relatively more stable than 0.95

Closer to unstability condition.

The Difference b/w value of βA ($|\beta A|$) at frequency where phase is 180° and ~~At~~ unity (0 dB).

→ Gain margin: The gain of the system at 180° phase shift.

→ Phase margin is 180° minus phase at 0dB

Barkhausen Criteria?

↳ $|\beta A| = 1$

↳ Overall phase shift = 0° or 360°

For self starting of oscillation βA should be kept greater than 1.

Oscillator?

Amplifier with positive feedback.

It does not require any external signal source.

It produces oscillations from its own DC.

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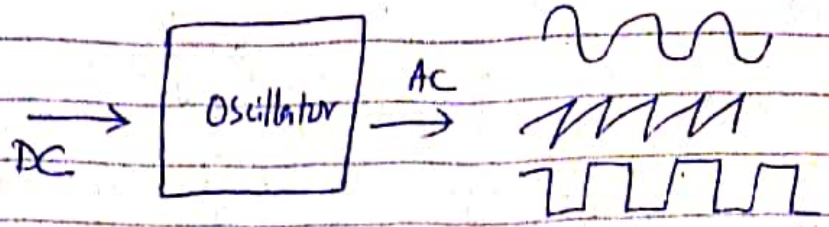
In other words it converts DC into AC.



Based on the o/p waveform, oscillators may be sinosidal or nonsinosidal / relaxation oscillators.

Oscillator requires two components
- amplifier
- Feedback network.

Sinosidal oscillators
- RC oscillator (in feedback)
- LC oscillator (in feedback)
- Crystal oscillator

The feedback network is a frequency selector. (Acts as a filter)

Two operations are performed by feedback network;
- Attenuation
- Desired phase shift at a particular frequency

frequency of operation ← resonant frequency.

Pole is that frequency at which the system transfer function becomes infinite.

Zero is that frequency at which the transfer function becomes zero.

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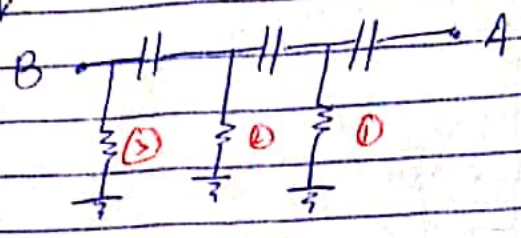
$Z = R - jX_c$

$Z = \sqrt{R^2 + X_c^2}$

$\text{Angle} = \tan^{-1}\frac{X_c}{R}$

$\tan 0° = 0$
$\tan 45° = 1$
$\tan 90° = \infty$

Problem with 2 RC sections ?



Point A to B overall phase shift must be 180° irrespective of the individual RC sections (may or may not be 60° each).

↳ due to loading effect.

How to overcome loading effect?

By using emitter follower circuit.

$$f = \frac{1}{2\pi RC\sqrt{2n}}$$

where n is the number of RC sections.

Section 1 is loaded by section 2.
section 2 by 3 & 1.
section 3 by i/p.
o/p by section 2

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To avoid loading effect o/p impedance of amplifier should be small than i/p impedance of the feedback network.

short circuit ⇒ Maximum loading effect.

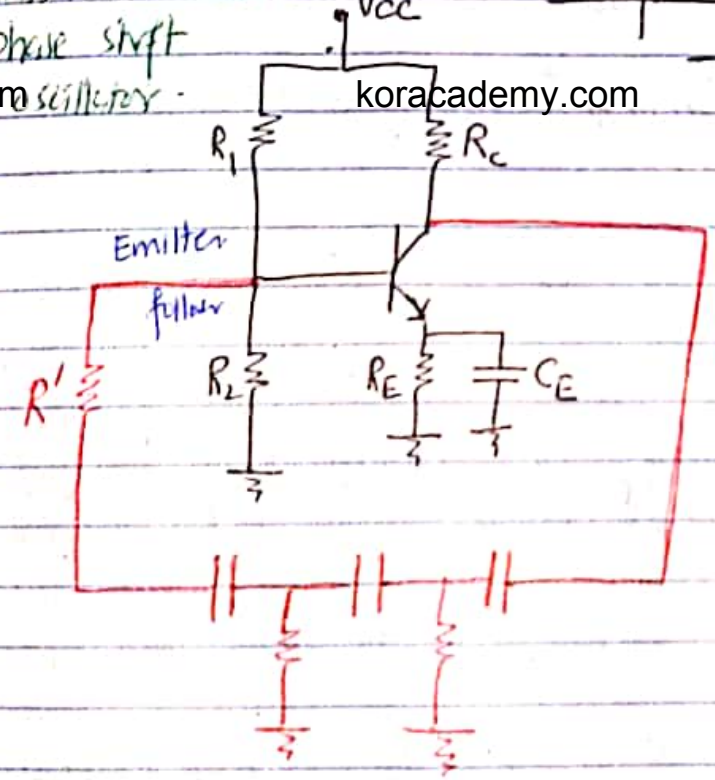
Amplifier → BJT → FET → Op Amp
BJT, FET → Discrete components
Discrete components ↔ Gain element.
Op Amp → IC

If βA < 1 we have clamped oscillation

To maintain constant amplitude oscillation, provide some continuity.

Practical version of Phase shift oscillator using npn BJT

This is a transistor phase shift oscillator.



Frequency
$\beta A = 1$
$f = 29$

To avoid loading effect place a emitter follower at the shown position.
↳ B/w amplifier and feedback network.

Bilal Register

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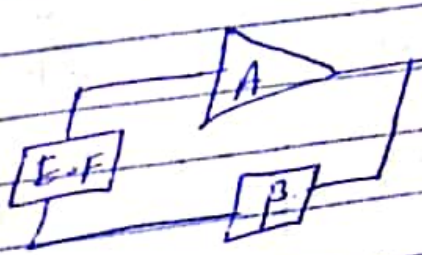
There are 4 hybrid parmeters.

h_{re} → Reverse voltage ratio = I/P / O/P
h_{fe} → Forward current ratio = O/P / I/P
h_{ie} → I/P impedance
h_{oe} → O/P impedance

Emitter follower is put for the purpose of impedance matching as a buffer.



The feedback signal is coupled at the base through 'R'.

Fc The frequency of oscillation is

$$f = \frac{1}{2\pi RC\sqrt{6+\frac{4R_c}{R}}}$$

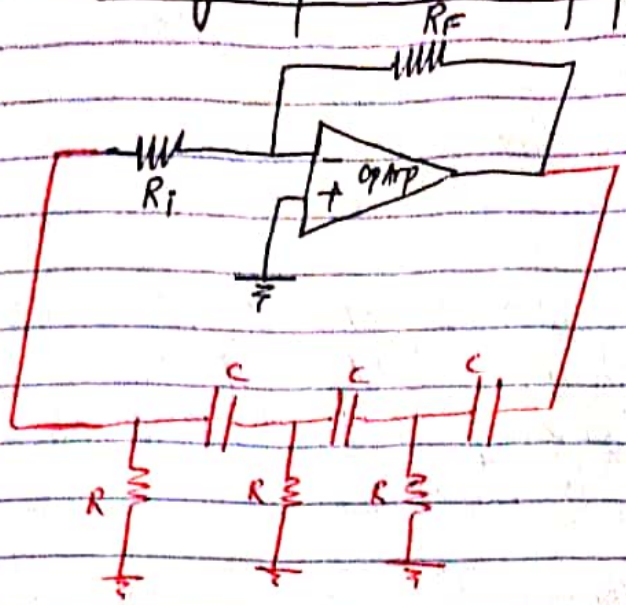
to 0

By To satisfy the condition
$|\beta A| = 1 \quad \beta A = 1$

$\angle \beta A = 0^\circ$ or 360°

$$h_{fe} > 23 + 29\frac{R}{R_c} + \frac{4R_c}{R}$$

Using Operational Amplifier.



$\beta A > 1$

$\beta = 1/29$

$A = 29$

$\beta A > 1$

$A > \frac{1}{\beta}$

$A > 29$

Amplifier

Feedback

Amplifier is connected in inverting configuration.

$\beta = \frac{1}{29}$ means o/p is attenuated 29 times.

$\frac{V_f}{V_o} = \frac{1}{29} \Rightarrow \boxed{V_f = \frac{V_o}{29}}$

The frequency of oscillation;

$f = \frac{1}{2\pi RC\sqrt{6}}$

At this frequency $\beta = \frac{1}{29}$ $\beta A = 1$

$A = 29$

Phase shift by feedback is 180°.

Wein Bridge Oscillator :

It is RC and sinusoidal oscillator.

It produces oscillation in the audio frequency range.

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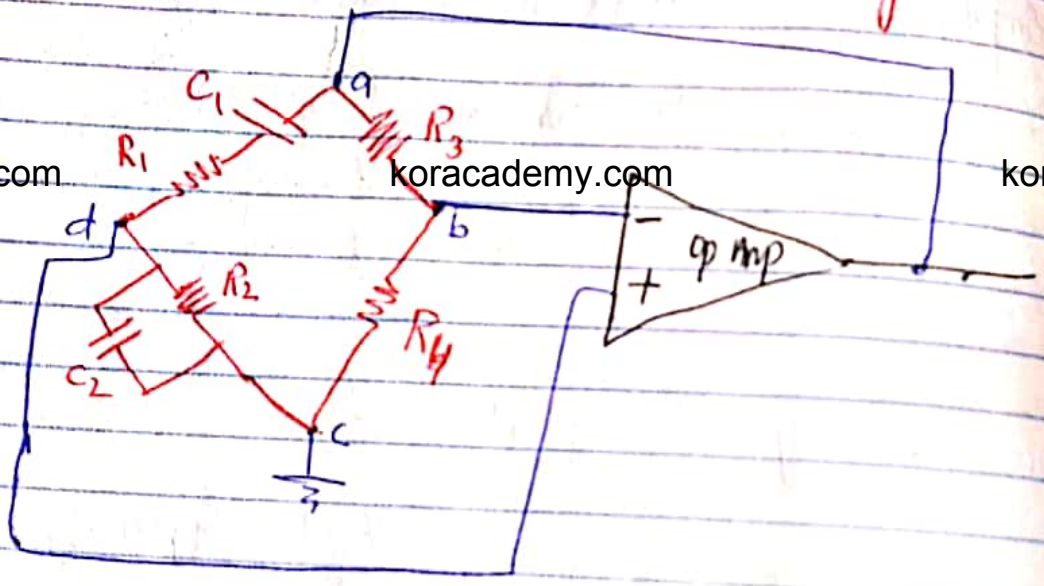
Low frequency oscillator 5 Hz to 500 kHz.
Low distortion - tunable.
High purity sine wave generator.
often used in lab work.

Practical version of this oscillator consists of Op Amp and RC bridge circuit. where the frequency of oscillation is set by R and C components.

We are not mentioned about the phase shift so we can use non inverting

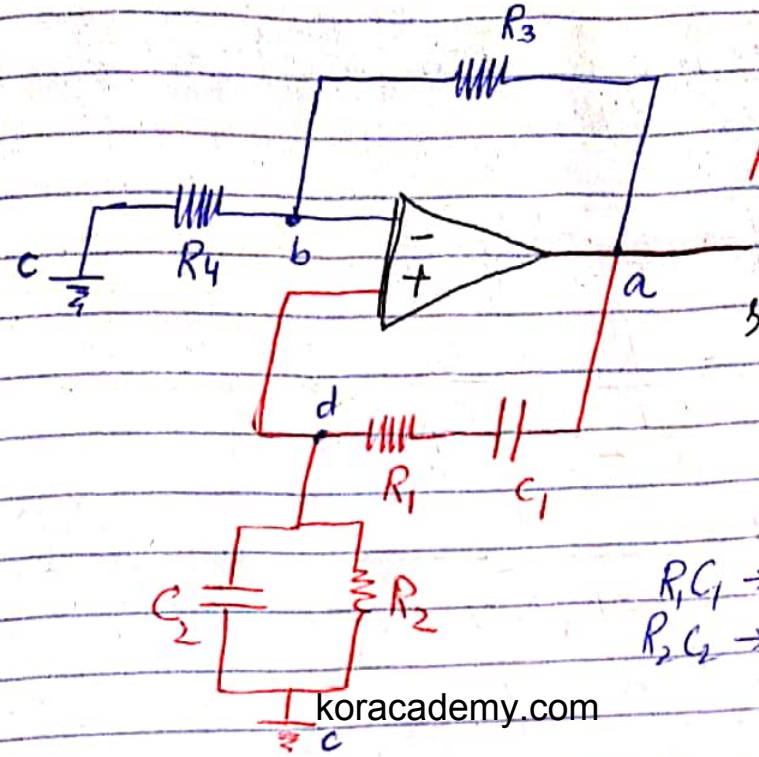


→ Resistors R_3 and R_4 determine the amplifier gain and are selected to make magnitude of the loop gain equal to 1 ie $|\beta A| = 1$.

→ R_1, R_2, C_1, C_2 are the frequency adjustment elements.

The op Amp o/p is connected at the bridge i/p at points a and c.

The bridge circuit o/p at points b and d is i/p to the op amp.

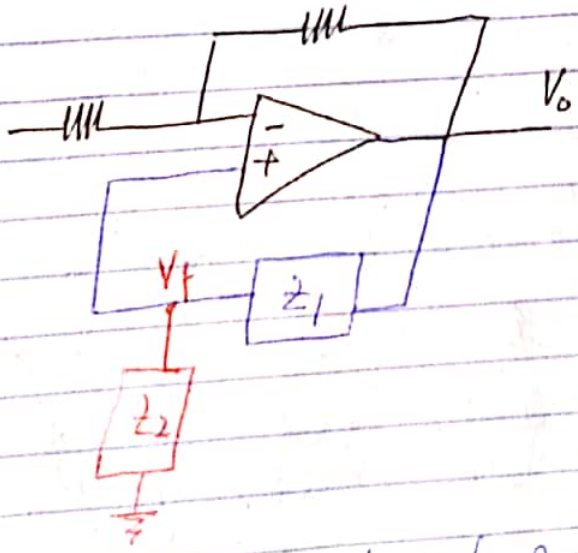


$A = 1 + \frac{R_3}{R_4}$

Sinusoidal o/p

R_1C_1 → high pass filter
R_2C_2 → Low pass filter.

Or



Combination of low and high pass filters; so it allows one intermediate frequency.

Called Lead Lagg filter

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$$V_f = \frac{Z_2}{Z_1 + Z_2} V_o$$

$$\beta = \frac{V_f}{V_o} = \frac{Z_2}{Z_1 + Z_2}$$

Combine low pass and high pass to get a band pass filter.

By performing analysis;

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

Also $$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$\Rightarrow f = \frac{1}{2\pi RC}$$

$$\frac{R_3}{R_4} = \frac{1}{1} + \frac{1}{1} = 2$$

$$A = 1 + 2 = 3$$

$\beta A > 1 \quad A > \frac{1}{\beta} \quad A > 3 \quad \beta = \frac{1}{3}$

$R_1 C_1$ provides equal and opposite phase shift to that provided by $R_2 C_2$.

↳ The result is 0°.

Normally C_1, C_2 are variable capacitors.

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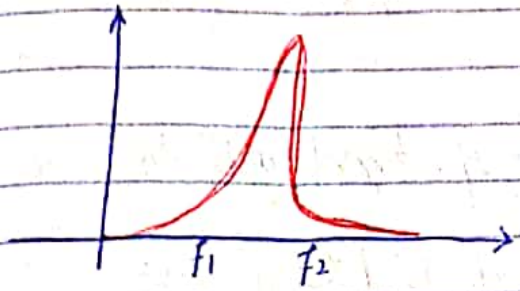
$X_C = \frac{1}{2\pi f C}$ $\quad X_C \uparrow \; f \downarrow$

At high frequencies C_1 and C_2 becomes short circuited $\Rightarrow V_f = 0 \quad \Rightarrow \beta = 0$

At low frequencies C_1 and C_2 are open circuited.
again $V_f = 0$, $\beta = 0$



$BW = f_2 - f_1$
↳ are allowed

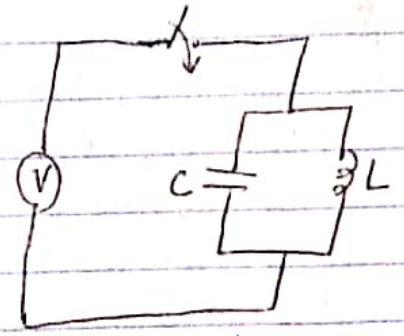
Tuned Oscillator Circuit
(tuned amplifier)

↳ allows only one particular frequency.

It is a filter followed by amplifier circuit.

They are sinusidal and high frequency oscillators.

LC Tank circut → parallel combination of L and C.



Initially switch closed; charge C to V then open switch.
Capacitor discharges through L. Initially current large and slowly decrease.
Now L will charge C again.
This charging and discharging provides oscillation.

Bilal Register

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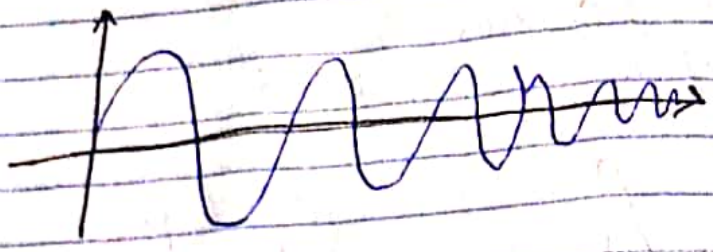
For ideal case we have sustained oscillations

But practically L has some resistance so I^2R loss

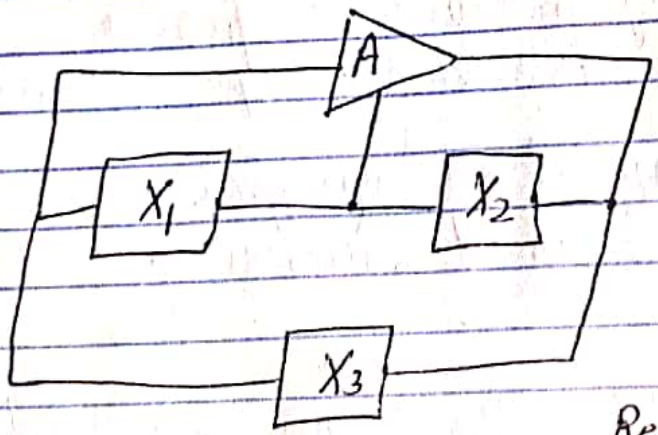
So we have damped oscillations.



We have a variety of tuned oscillator circuit available.

The feedback network is LC Resonant tank circuit (which is a frequency selective network)

The basic configuration is as:



Oscillator Type	Reactance elements		
	X_1	X_2	X_3
Colpitts oscillator	C	C	L
Hartley oscillator	L	L	C
Tuned i/p tuned o/p	LC	LC	-

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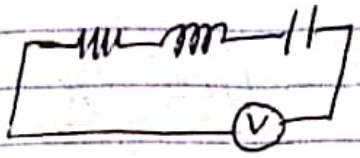
Colpit osc is the electrical dual of Hartley oscillator.

At Resonant frequency f_o; $X_L = X_C$

$$2\pi f_o L = \frac{1}{2\pi f_o C}$$

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$



At resonance

$$Z = R + j(X_L - X_C)$$

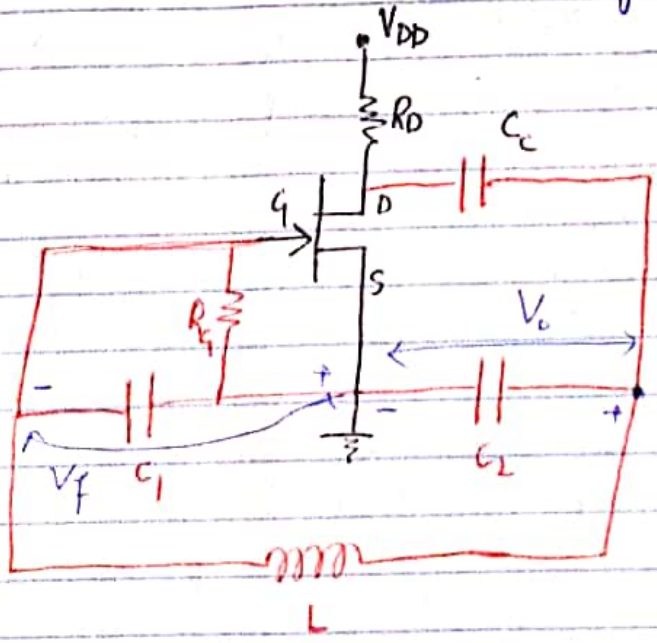
$$\Rightarrow Z = R$$

↳ mmmm impedance.

Parallel combination provides infinite impedance

Colpitts Oscillator:

using FET.



Bilal Register

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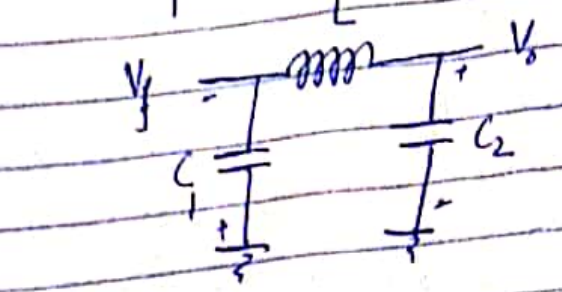
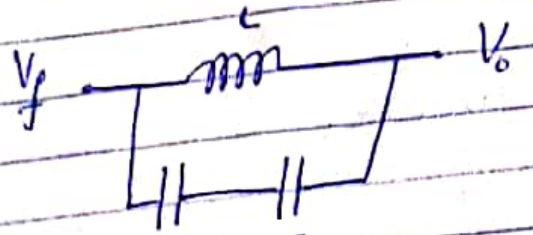
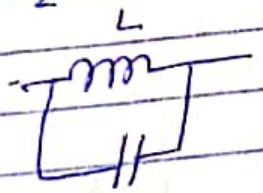
The feedback network;



$$Z = \frac{jX_L(-jX_{C_1} - jX_{C_2})}{jX_L - jX_{C_1} - jX_{C_2}}$$



$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$$



$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

Ideally, At resonance the impedance of a tank circuit is infinite.

$$Z = \frac{jX_L(-jX_{C_1} - jX_{C_2})}{jX_L - jX_{C_1} - jX_{C_2}} = \infty$$

$$jX_L - jX_{C_1} - jX_{C_2} = 0$$

$$X_L = X_{C_1} + X_{C_2}$$

$$\omega_0 L = \frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2}$$

$$\omega_0^2 = \frac{1}{L}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)$$

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$$= \frac{1}{L}\left(\frac{C_1 + C_2}{C_1 C_2}\right) = \frac{1}{L C_{eq}}$$

$$\omega_0 = \frac{1}{\sqrt{L C_{eq}}}$$

$$\Rightarrow f_0 = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

$$V_0 = I X_{C_2} = \frac{I}{2\pi f C_2}$$

$$V_f = -I X_{C_1} = -\frac{I}{2\pi f C_1}$$

$$\beta = \frac{V_f}{V_0} = -\frac{I X_{C_1}}{I X_{C_2}} = \frac{-X_{C_1}}{X_{C_2}}$$

$$\Rightarrow \boxed{\beta = -\frac{C_2}{C_1}}$$

$$\beta A = 1 \qquad A = \frac{1}{\beta} \qquad \boxed{A = -\frac{C_1}{C_2}}$$

For self starting of oscillation $A \geq \frac{C_1}{C_2}$

$$|A| > \frac{C_1}{C_2}$$

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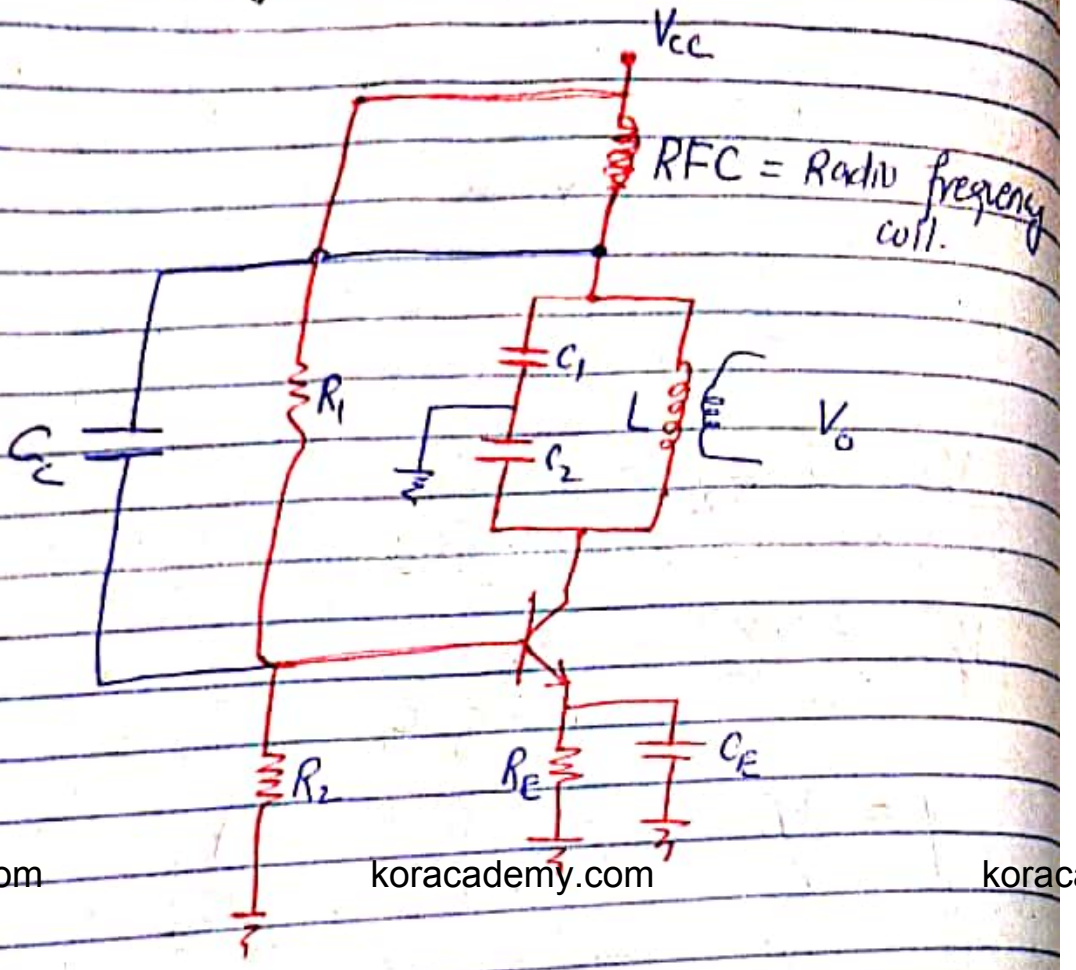
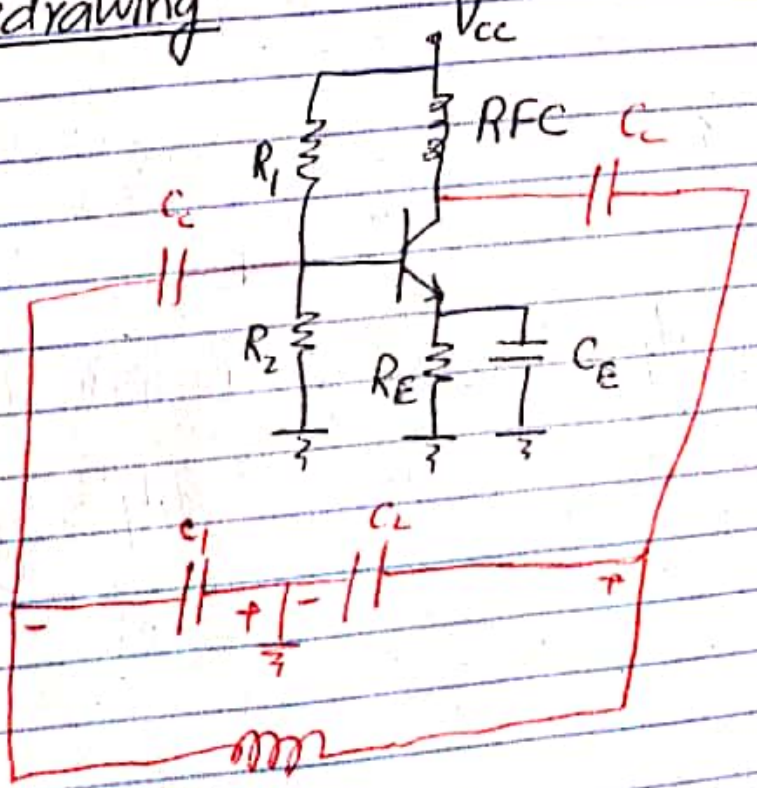
Using BJT



Redrawing



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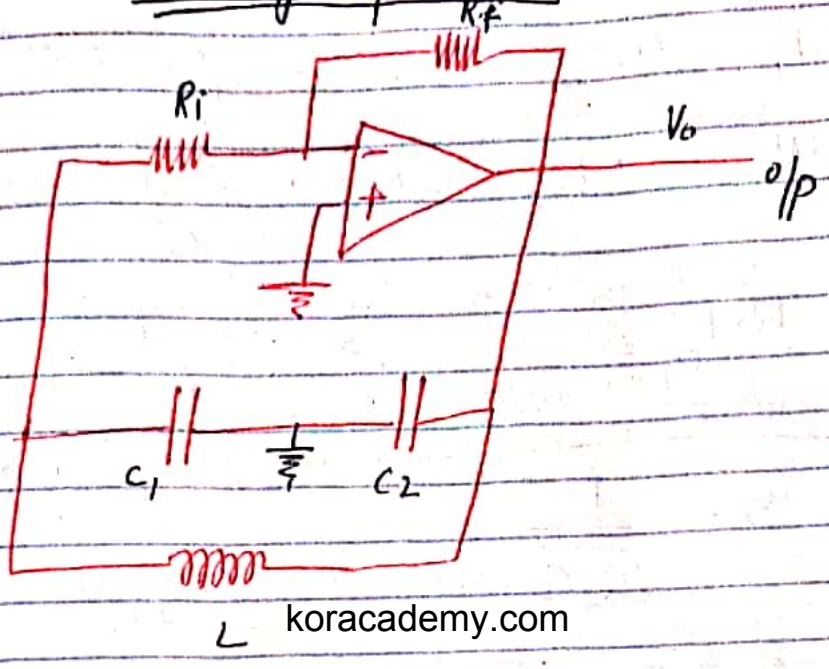
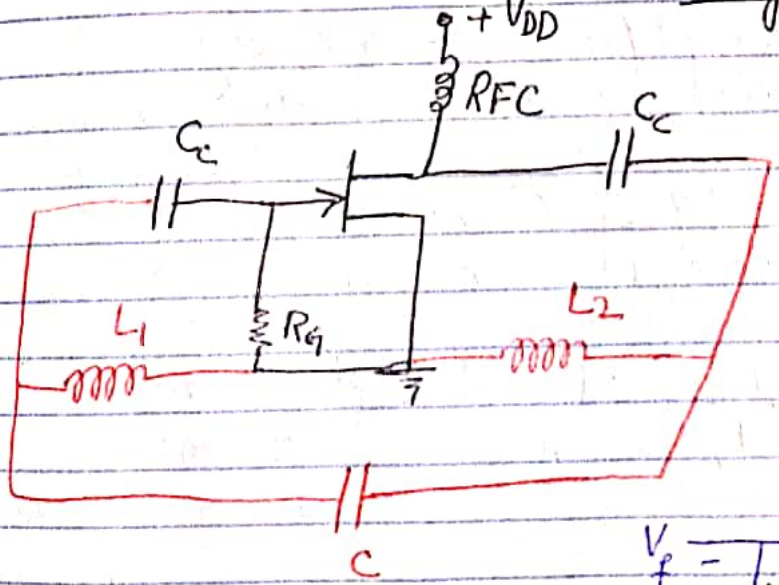
The transistor provides 180° phase shift and so does the tank LC unit so the overall phase shift is 0° or 360°.

Using Op Amp

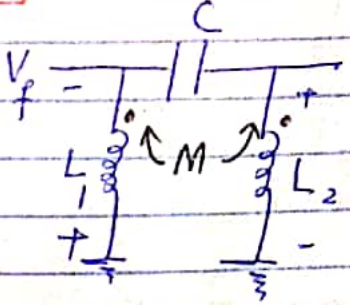


Hartley Oscillator

Using FET



V_o and V_f are out of phase by 180°.



Inductors in series;

$$L_{eq} = L_1 + L_2 + 2M$$

Bilal Register

Date: / /

$$Z = \frac{\left(j\omega L_1 + j\omega L_2 + j\omega 2M\right) - \frac{j}{\omega_c}}{j\omega L_1 + j\omega L_2 + j\omega 2M - j/\omega_c}$$

At resonance $Z \approx \infty$

$$\Rightarrow j\omega L_1 + j\omega L_2 + j\omega 2M - j/\omega_c = 0$$

$$\omega_0 (L_1 + L_2 + 2M) = \frac{1}{\omega_0 C}$$

$$\omega_0 L_{eq} = \frac{1}{\omega_0 C} \quad \Rightarrow \omega_0^2 = \frac{1}{L_{eq} C}$$

$$\boxed{\omega_0 = \frac{1}{\sqrt{L_{eq} C}} \Rightarrow f_0 = \frac{1}{2\pi\sqrt{L_{eq} C}}}$$

Lecture 7 06/1/20

Normally in amplifier circuit especially in inverting amplifier overall phase shift is 180°

For oscillator it is 0° or 360° or integral multiple of 360° or 2π radians.

Based on the components used in the feedback circuit, we name the oscillators.

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CRYSTAL OSCILLATOR

- Tuned oscillator circuit.
- Has a piso electric circuit and a resonant tank circuit in the feedback loop to control the frequency of oscillation.

The available piso electric materials are;
→ Rochelle salt
→ Tourmaline
→ Quartz → most frequently used.

Reasons behind variation of frequency?
- change in supply voltage
- change in temperature and climate.
- change in the components.

How is crystal oscillator different?
- It provides a highly stabilized frequency of oscillation.
- Quality factor is very high.
- Less expensive.
- Highly available in nature.
- Robust (mechanically strong)

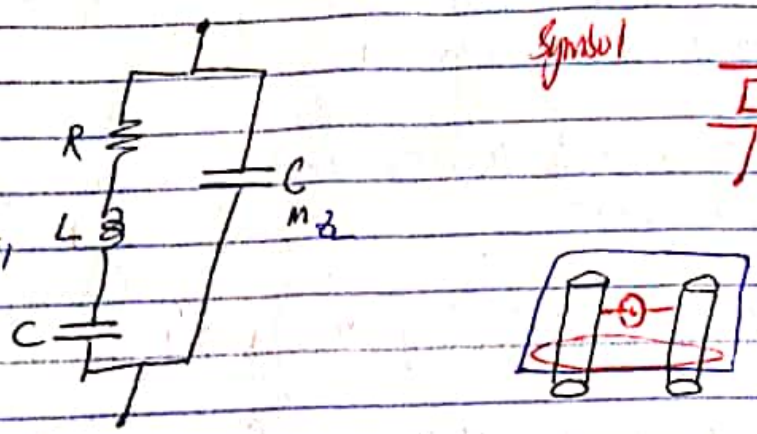
Piso electric effect?
When mechanical stress / force is applied on the crystal, an emf is developed.

Inverse piso electric effect.
When emf is applied, mechanical distortion is produced.

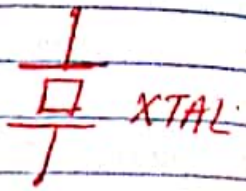
Date: __/__/__

The maximum frequency that we can get from a crystal is its natural resonant frequency.

The electrical equivalent circuit is as;



Symbol



R: Internal friction of the crystal and it should be minimum so that losses due to R should be minimum.

L, C: These represent electrical equivalent of crystal. L corresponds to mass and C corresponds to

Crystal has electromechanical resonance.

Q factor is very high. Q ↑ ⇒ losses ↓

The greatest vibration occurs at the crystal natural frequency which depends on physical dimension of crystal and on the way it is cut.

Normally $f \propto \frac{1}{\text{Thickness}}$

C_m: Capacitance due to mechanical mounting.

Date: / /

There are two resonant modes of operation.
(i) Series resonance (ii) Parallel resonance.

Impedance of series RLC arm is,

$$Z_1 = R + j\omega L - \frac{j}{\omega C}$$

Series Resonance occurs at a low frequency.

At resonance, Z is minimum

$$\omega_r L = \frac{1}{\omega_r C} \Rightarrow \omega_r^2 = \frac{1}{LC}$$

$$\Rightarrow f_r = \frac{1}{2\pi\sqrt{LC}}$$

For parallel resonance:
Neglect R as it is very small as compared to Q factor.

$$Z = \frac{Z_1 Z_2}{Z_1 + Z_2}$$

$$Z = \frac{\left(j\omega L - \frac{j}{\omega C}\right)\left(-\frac{j}{\omega C_m}\right)}{j\omega L - \frac{j}{\omega C} - \frac{j}{\omega C_m}}$$

For parallel resonance, impedance is maximum.

$$j\omega L - \frac{j}{\omega C} - \frac{j}{\omega C_m} = 0$$

$$\omega_r L = \frac{1}{\omega_r C} + \frac{1}{\omega_r C_m} \Rightarrow \omega_r^2 = \frac{1}{L}\left(\frac{1}{C} + \frac{1}{C_m}\right)$$

$$\omega_r = \frac{1}{\sqrt{LC_{eq}}} \qquad f_r = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

Bilal Register

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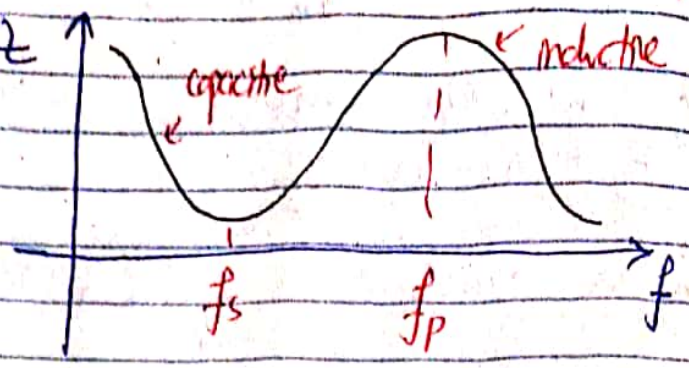
Parallel resonance occurs at a high frequency.

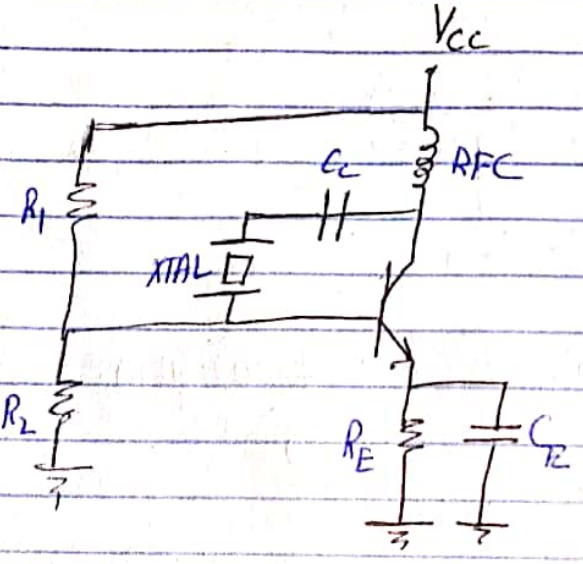


Circuit operating frequency is set by crystal operating frequency.

Series Resonant Circuit

The crystal is connected as a series element in the feedback path.

Impedance ↓ ⇒ maximum feedback signal is available.



This is a common emitter amplifier with voltage divider biasing.

RFC allows DC current and not AC.

Bilal Register

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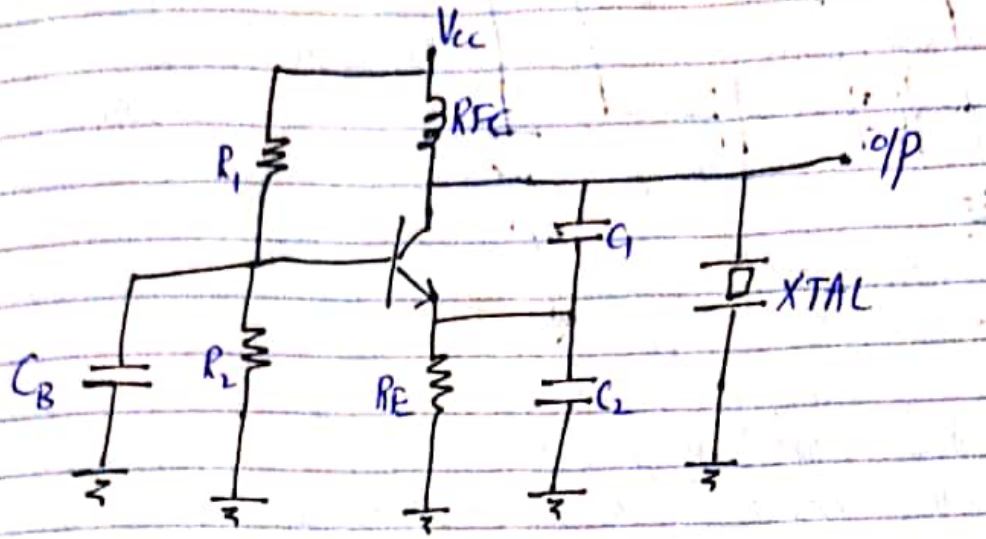
Parallel Resonant Circuit

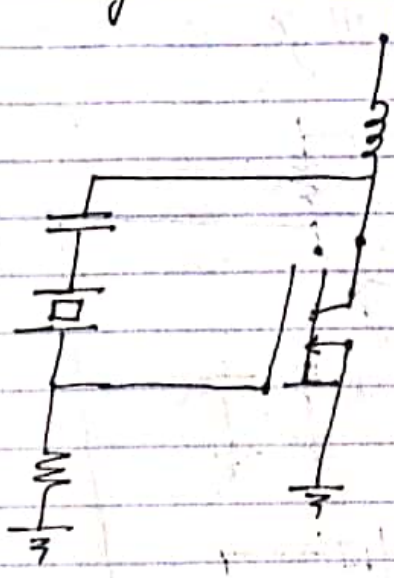
Impedance is very high and is connected in parallel.

At parallel resonant frequency, the crystal appears as an inductive reactance of a large value.



This is a common base configuration.
↳ A modified version of colpitt oscillator.

Fig 14.33 Using MOSFET.



This is an n channel D mosFET.

Fig 14-35 → Miller crystal oscillator.

Bilal Register

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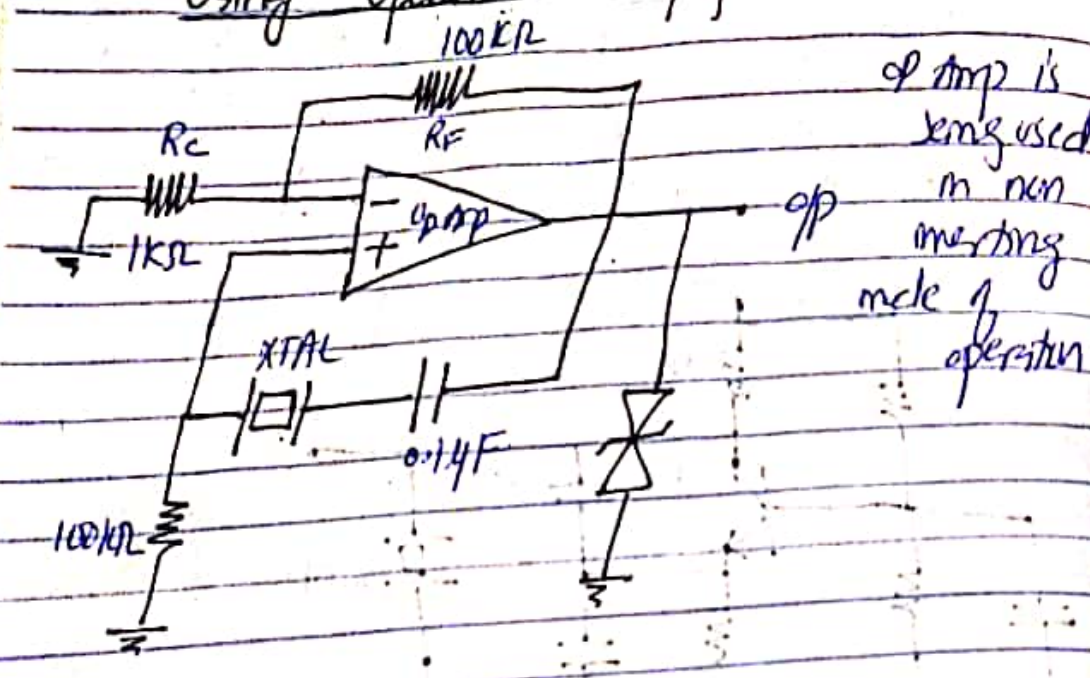
Using Operational Amplifier



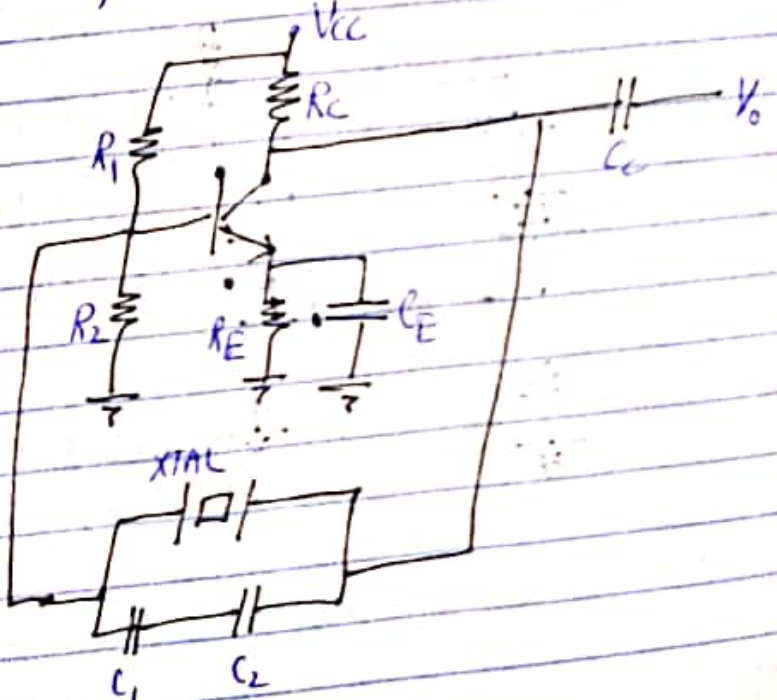
op amp is being used in non inverting mode of operation.

- The gain B is very large
- The result is a square wave.

$$A = 1 + \frac{R_E}{R_C} = 1 + \frac{100}{1} \Rightarrow A_f = 101$$

A pair of zener diode is connected at output to provide output voltage as zener voltage.

Another circuit for parallel resonance mode →



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Gain may be greater than 1 but efficiency is always less than 1.

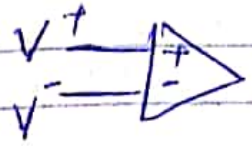
555 timer (Floyd Book)

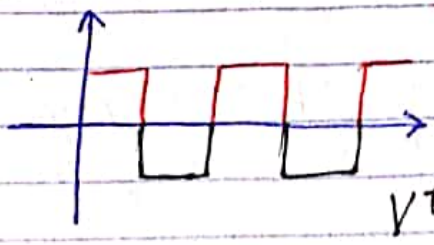
- It is analogue digital IC.
- It is a versatile IC with many applications.
- It can be operated in astable, monostable and bistable modes of operation.

- 555 timers provide relaxation oscillations.

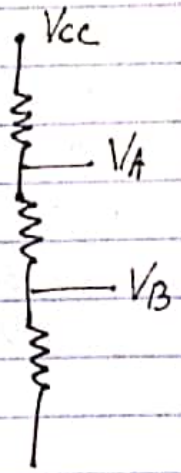
- It consists of two comparators, 1 flipflop, 1 discharge transistor and a resistive voltage divider.

Operation of Comparator;





FF → bistable multiple vibrator.



$$V_A = \frac{5+5}{15} V_{cc} = \frac{10}{15} V_{cc}$$

$$V_A = \frac{2}{3} V_{cc}$$

$$V_{13} = \frac{5}{15} V_{cc} = \frac{1}{3} V_{cc}$$

Bilal Register

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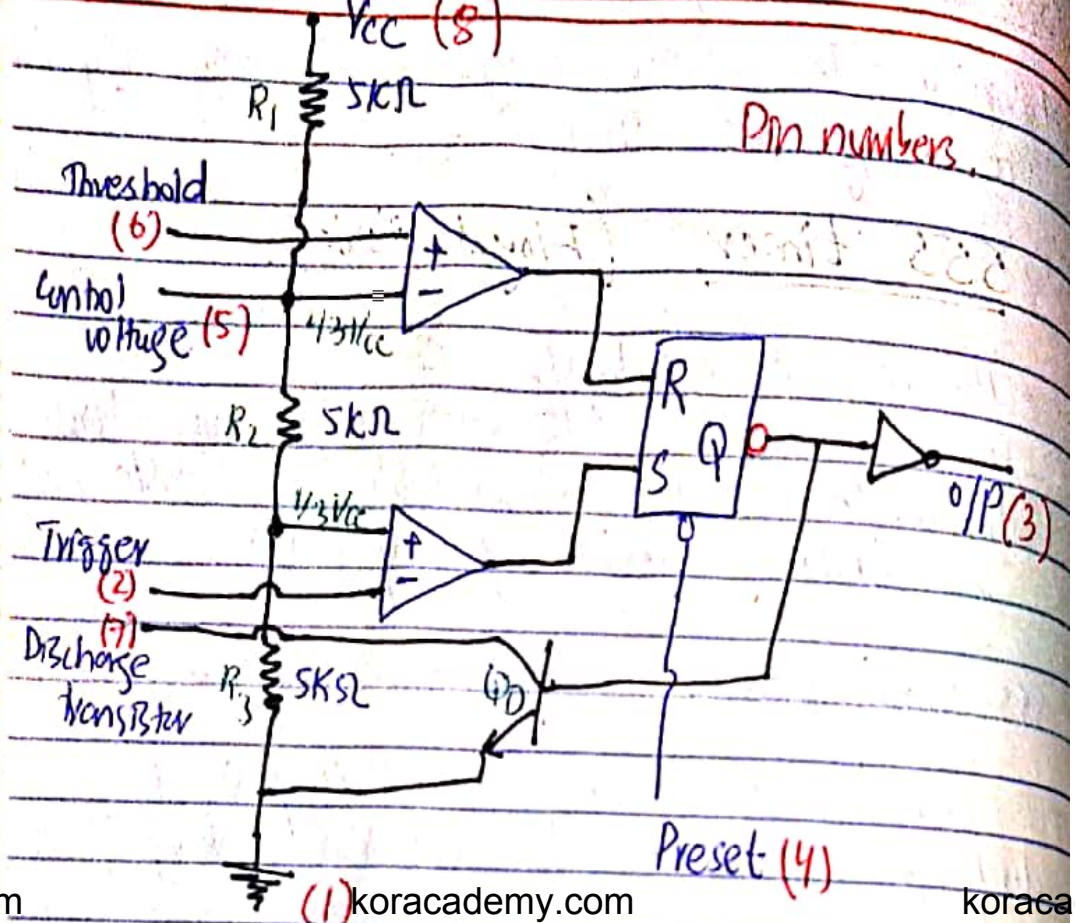

When the trigger voltage goes 1/3 Vcc the FF sets and the o/p jumps to high level.

The threshold i/p is normally connected to an external RC timing circuit.

When the external capacitor voltage exceeds 2/3 Vcc, the upper comparator resets the ff.

→ which in turn o/p is low
lower comparator sets ff → o/p is high

→ The discharge transistor Q_D is turned ON and provides a path for discharge of

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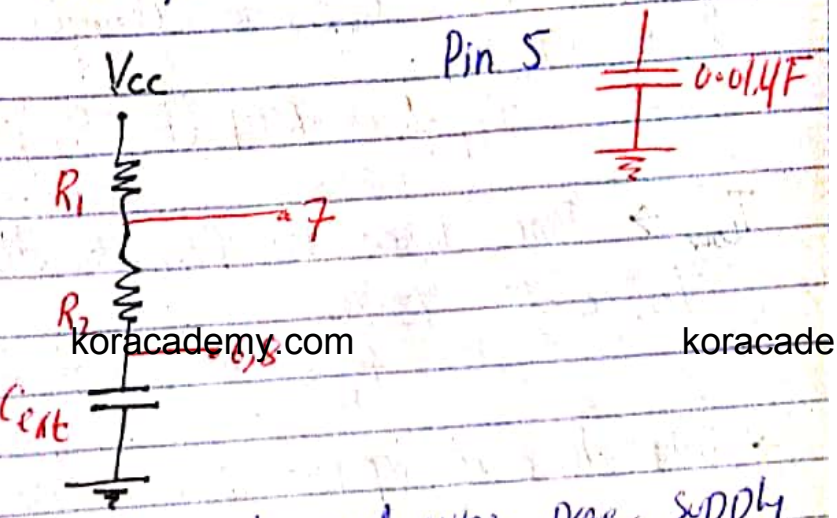
Astable Operation

- No stable
- Also called free running multivibrator and is a square wave osullator.

→ Pin 6 and 2 are connected together.
Pin 1 is grounded. Pin 4 is Vcc.
R_1, R_2 and C_{ext} form the timing circuit.



Initially C_{ext} is uncharged when power supply is turned ON and the trigger voltage is at 0V.
o/p of upper comparator is low.

C_{ext} charges through R_1 and R_2 and discharges through R_2 and transistor.

DIP → dual inline package
↳ on both sides we have pins.

SIP → single inline package
↳ pins on one side.

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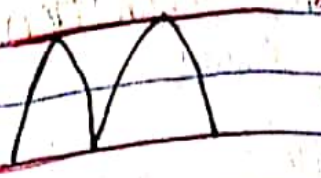
Capacitor voltage



Duty cycle = $\frac{t_{ON}}{T}$

→ The time that the o/p is high (T_H is how long it takes C_{ext} to charge from 1/3 Vcc to 2/3 Vcc.

$$t_H = 0.694 (R_1 + R_2) C_{ext}$$

T_{low} → Time taken by C_{ext} to discharge from 2/3 Vcc to 1/3 Vcc

$$t_L = 0.694 \, R_2 \, C_{ext}$$

→ Total time of o/p waveform is sum of t_H and t_L

$$T = t_H + t_L = 0.694 (R_1 + 2R_2) C_{ext}$$

→ The frequency of oscillation, $f = \frac{1}{T}$

$$f = \frac{1.44}{(R_1 + 2R_2) C_{ext}}$$

To make duty cycle 50% ?

Make charging and discharging time equal ie R_2 should be very large than R_1

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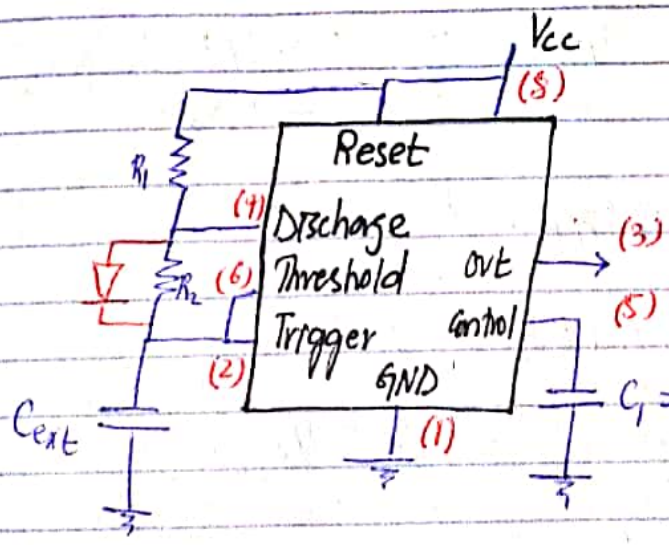
$$\text{Duty cycle} = \frac{t_H}{T} \times 100\% = \frac{0.694 (R_1 + R_2) C_{ext}}{0.694 (R_1 + 2R_2) C_{ext}}$$

$$= \frac{R_1 + R_2}{R_1 + 2R_2} \times 100\%$$

For duty cycle less than 50% the circuit can be modified in such a way that charging takes place only through R_1 and discharging only through R_2.

How? Connect a diode across R_2 such that during charging diode is forward biased and R_2 is bypassed.

During discharging diode will be R.B and capacitor will charge through R_2 and transistor Q_D.



Now $t_H = 0.694 R_1 C_{ext}$

$t_L = 0.694 R_2 C_{ext}$

$T = 0.694 (R_1 + R_2) C_{ext}$

$D = \frac{t_H}{T} = \frac{R_1}{R_2}$

Bilal Register

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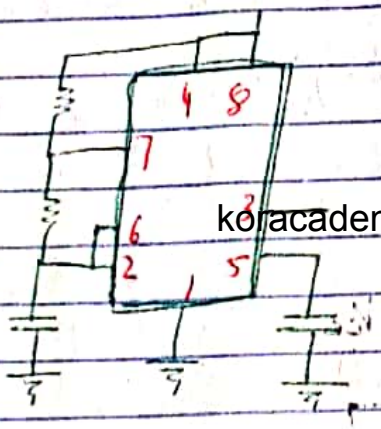
Why free running?
B/c no external signal at all.

Example 1. A 555 timer with $R_1 = 2.2k\Omega$, $R_2 = 4.7k\Omega$, $C_{ext} = 0.022\mu F$. Determine the frequency of o/p and duty cycle. Diode is not connected.

$f = 5.64\ KHz$ $D = 59.5\%$

Example 2 Determine the frequency and draw the o/p waveform for circuit with $R_1 = R_2 = 7.5k\Omega$, $V_{cc} = 5V$, $C_{ext} = 0.1\mu F$ and diode is not connected.



$$f = \frac{1.44}{(R_1 + 2R_2)C_{ext}}$$

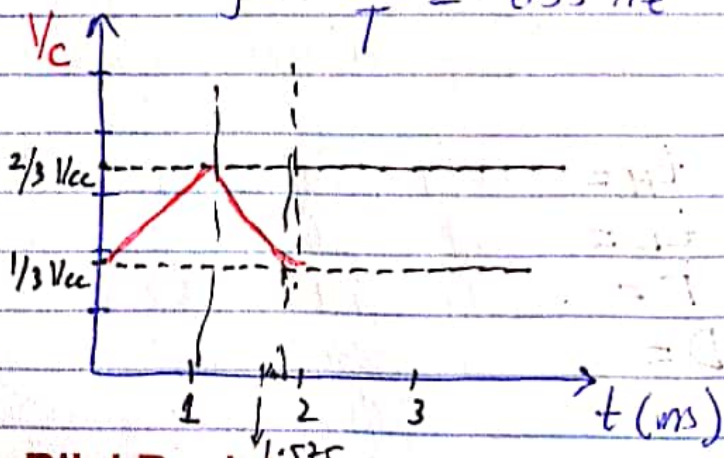
$f =$ _____

$T_H = 0.694(R_1 + R_2)C_{ext}$
$= 1.05\ ms$

$T_L = 0.694\ R_2\ C_{ext} = 0.525\ ms$

$T = t_H + t_L = 1.575$

$f = \frac{1}{T} = 635\ Hz$



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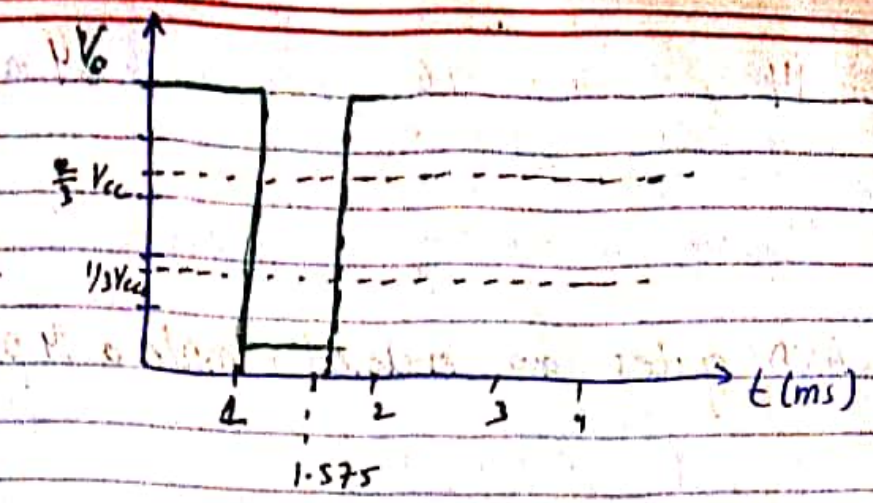

Monostable

- Mono → one / single state.
- Device stable in one state.
- No oscillation.
- We need to trigger it externally.

Lecture 8 13/01/20

Digital Logic Families

(DLD Morris Manno book)

Digital circuits are constructed from ICs.

An integrated circuit is a small silicon semiconductor crystal called a chip containing the electronic components for constructing logic gates.

Various gates are connected inside the chip to form the IC. The chip is mounted on a ceramic or plastic container and connections are welded to external pins to form the integrated circuit. The number of pins may range

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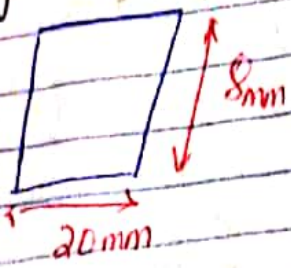
from 14 in a small IC package to 64 or more in a larger package.

The size of IC package is very small.

eg 4 AND gates are enclosed inside a 14 pin IC



Each IC has a numeric designation printed on the surface of package for identification.

Manufactures provide data books (catalogs) and internet websites that contain discription and information about the IC they manufacture.

Chapter 10
↳ Digital Integrated Circuits (Morris Mano)

Levels of Integration.

We classify digital ICs in terms of circuit complexity which is measured in terms of number of logic gates in a single package.

i) Small Scale Integration (SSI)

→ Few independent gates in a single package.

The number of gates is usually less than 10.

I/P and o/p are connected to the pins.

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It is limited by the number of pins available on the IC.

(ii) Medium Scale Integration (MSI)

It contains approximately 10 to 1000 gates per IC. It performs specific digital elementary operation.

MSI digital functions are decoder, adder, register, mux, counters.

(iii) Large Scale Integration (LSI)

Contain 1000s of gates in a single package.

They include digital systems such as processor, memory chips and programmable logic devices.

(iv) Very large scale integration (VLSI)

Contains 100,000s of gates in a single package.

→ Complex microprocessor chips

Because of their small size and low cost VLSI devices have revolutionized the computer system design technology, giving the designer the ability to creat ----

Digital Logic Families

How we categorize digital ICs?

(i) Circuit complexity

(ii) Logical operation.

(iii) Circuit technology (how we build the IC)

Bilal Register

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The circuit technology is refered to as digital logic family and each logic family has its own basic electronic circuit.

The basic electronic circuit in digital IC is NAND, NOR or an inverter gate.

Classification of Digital Logic Families

We have two devices;

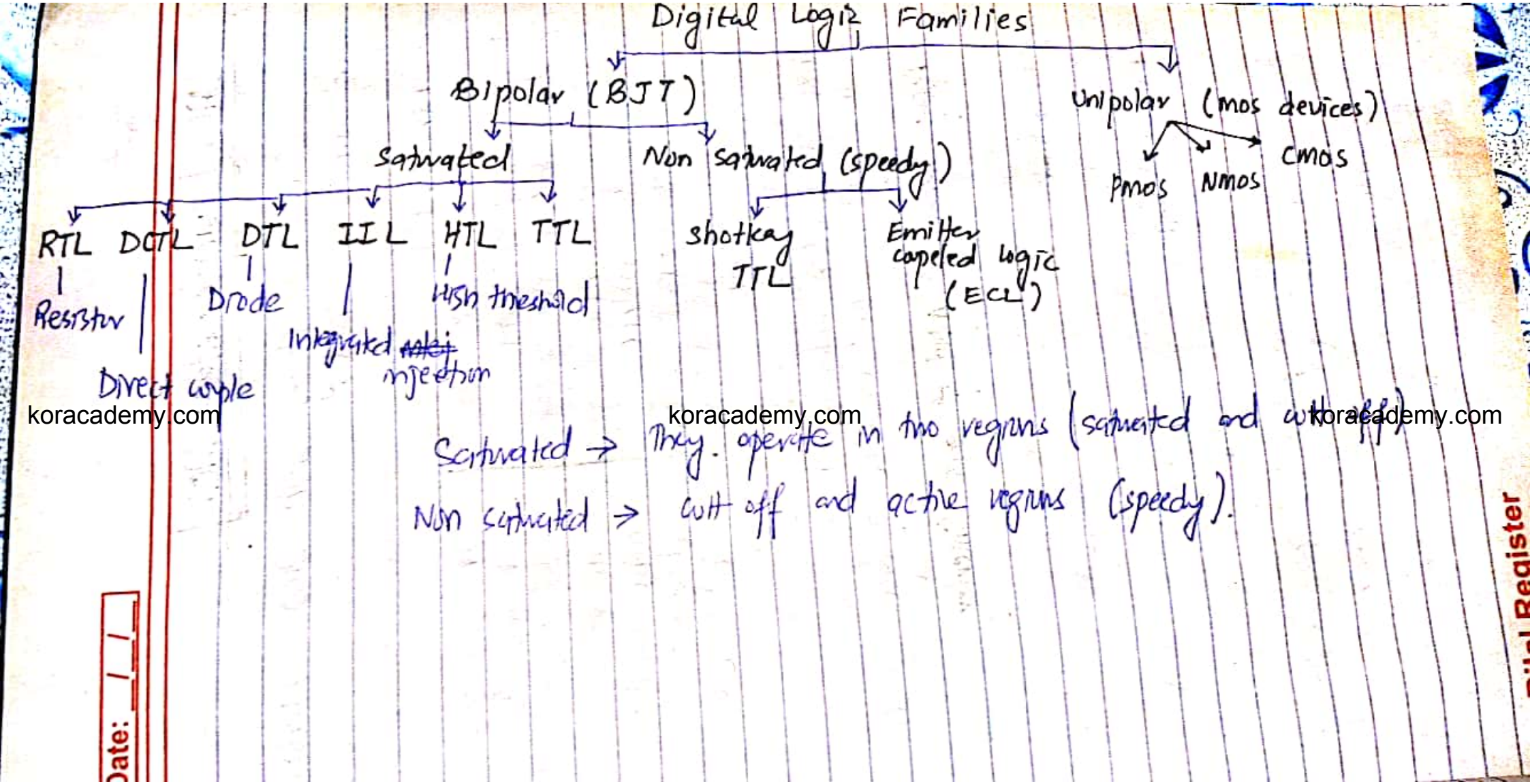
(i) Bipolar devices (BJT)

(ii) Unipolar devices (FET) (specially EMOSFET)

Mos device means MOSFET.

Mos

CMos PMOS NMOS



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CMOS [Complementary MOS]

CMOS: consists of both PMOS and NMOS on same substrate.

Characteristics:

i. Speed of operation.
ii. Power dissipation
iii. Figure of merit.
iv. Current and voltage parameters.

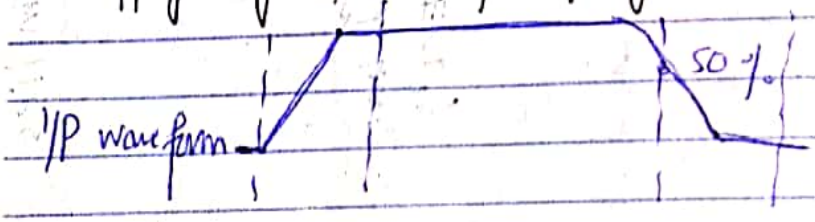
↓ book

Power supply requirement.

Fan out
noise immunity
and flexibility
available

More propagation → less speed delay.
Most of the time we take average speed

Apply signal at input of gate (inverter)



Propagation delay is taken as the average of these two times (t_{PHL} and t_{PLH})

$$\text{Time} = \frac{t_{PHL} + t_{PLH}}{2}$$

$t_{PLH} > t_{PHL}$

Bilal Register

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Power dissipation

Amount of power dissipated in IC.

It is measured in milliwatts.

Figure of merit.

- Product of power and speed.

Speed → in terms of propagation delay time.

expressed in nanoseconds.

Figure of merit = Propagation delay time (ns) × Power (mW)

= PJ

A low value of figure of merit is desirable.

When we increase speed so power dissipation also increases and vice versa.

Fan out ? It is the number of similar gates which can be driven by a gate.

High fan out is advantageous. b/c it reduces the need of additional drivers to drive more gates.

Current And Voltage Parameters.

High level i/p current.

Noise immunity :-

Noise → unwanted electrical signal.

↳ It is the circuit ability to tolerate noise

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signal without affecting o/p of the gate.

Quantitative measurment of noise immnity is called noise margin.

Two types of noises;
DC Noise, AC noise.

Whenever current flows trough circuit it produces noise called thermal noise (Johson).

Proper power supply voltages are required for a particular IC.

Fan out : Number of standard loads connected to IC.

Load → anything that draws current.

Noise marjin.
Maximum external noise voltage added to an i/p signal that does not cause an undesirable change in circuit output.

Fan IN. No. of inputs available in a gate.

Two major applications of transistor (BJT, FET).
(i) Amplification
(ii) Switching.

-ve logic and +ve logic.

Bilal Register

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Two voltage levels.

High voltage level Low voltage level.

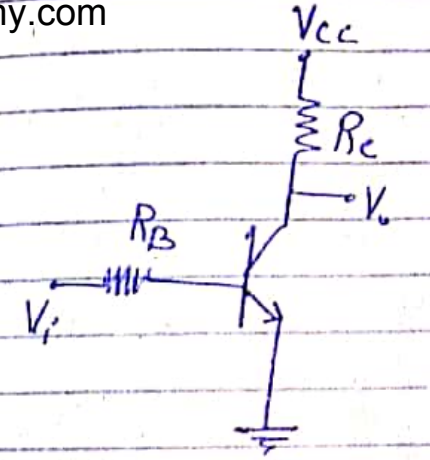
Logic 0 → low level voltage
Logic 1 → High level voltage
} +ve logic

Logic 0 → High level voltage
Logic 1 → low level voltage
} -ve logic

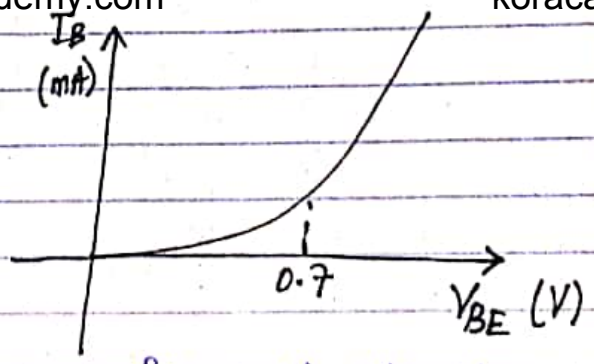
PMOS operates on -ve logic.
NMOS operates on +ve voltage.

Transistor As A Switch

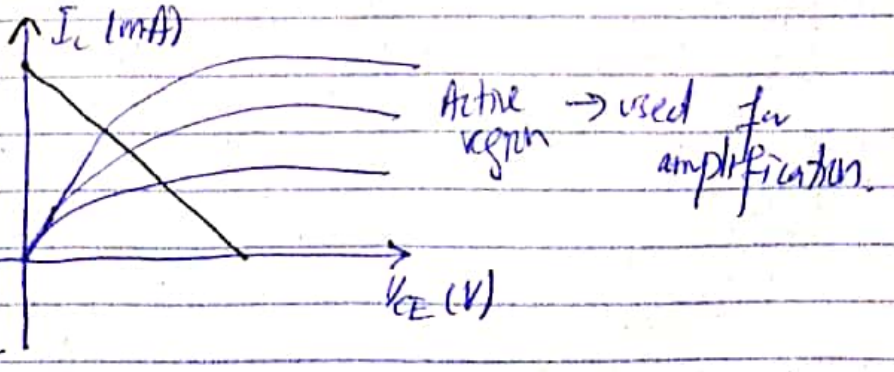
Most of time transistor is NPN.



common emitter configuration.



Base emitter characteristics.



collector emitter characteristics

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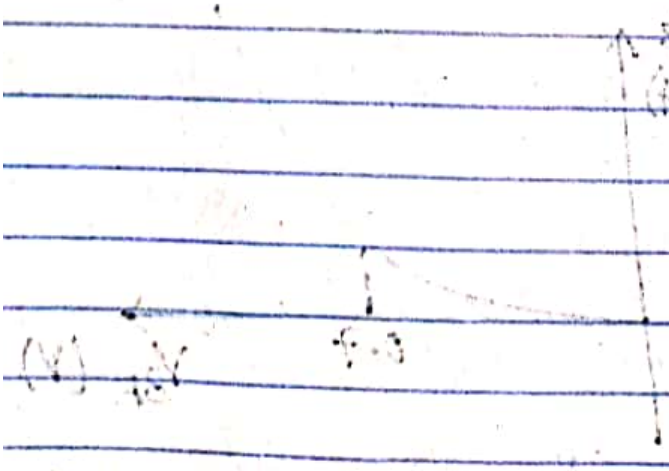
For switching purpose we use saturation and cut off region.



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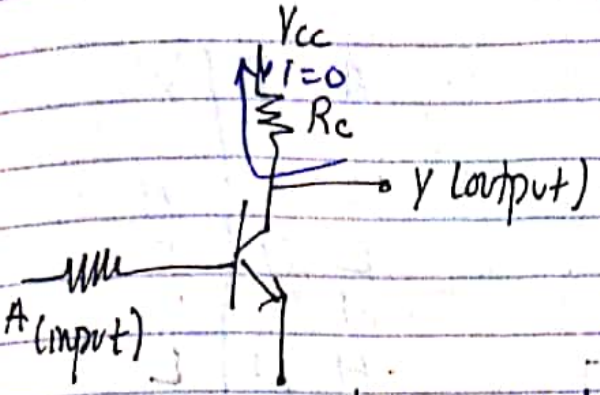
Logic Families

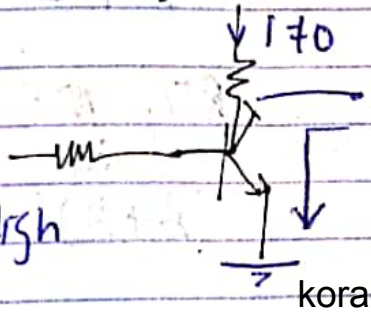
① Resistor transistor logic (RTL)

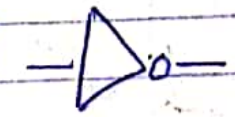
npn → I_b → logic high → transistor ON.

short circuit

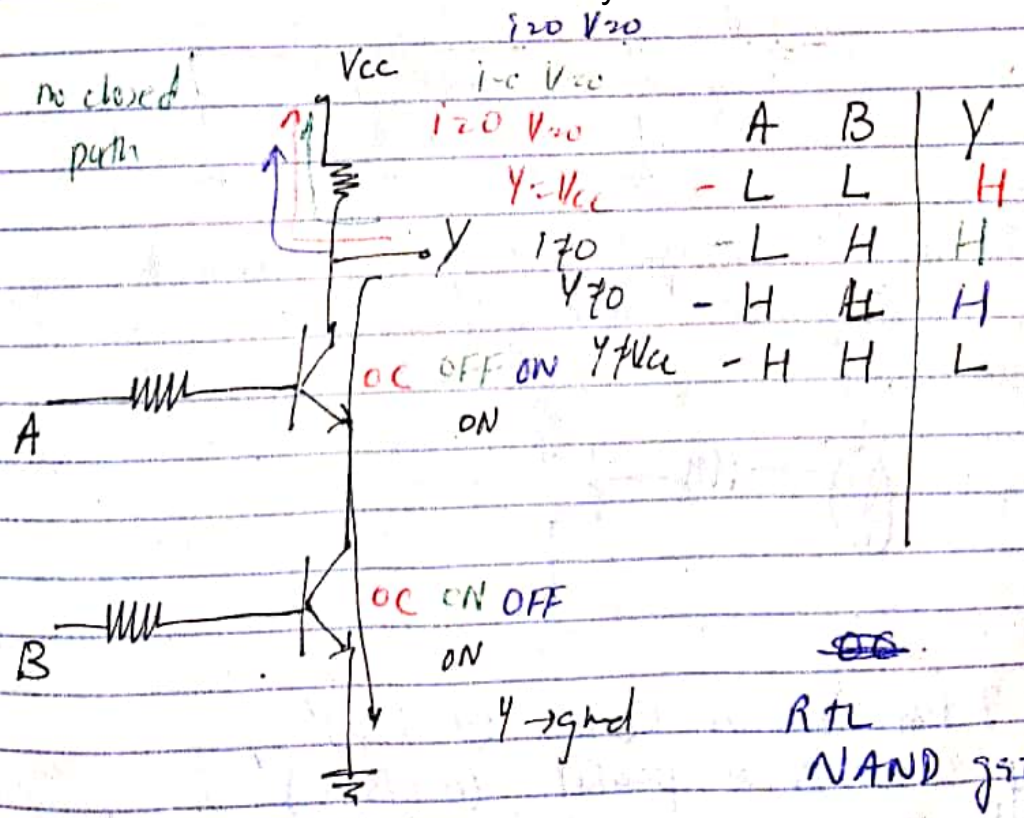


Input (A)	Output (Y)
Low	High.
High	low.





Inverter / Not gate.



A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

RTL NAND gate.

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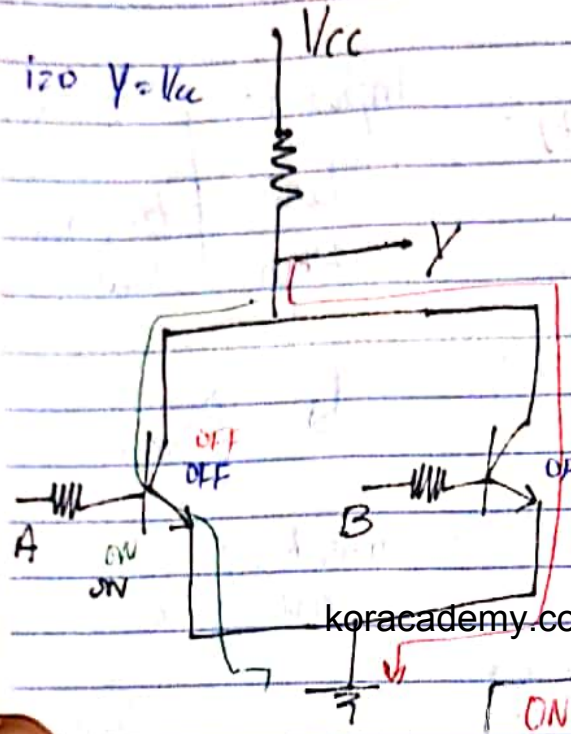
To make an AND gate at o/p connect NAND output to an inverter.

$(\overline{A \cdot B})' = A \cdot B$

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L



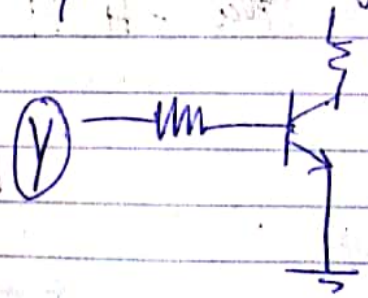
i.e. Y = Vcc

RTL NOR Gate

$(A+B)'$

ON → transistor SC
OFF → transistor OC

To make OR gate at o/p A, connect NOR o/p to NOR gate.

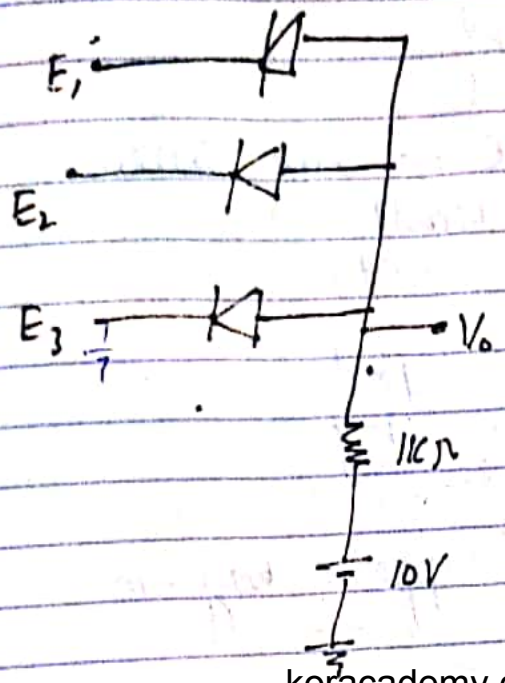


→ If 3 transistors in series $(A \cdot B \cdot C)'$
→ If 3 transistor in parallel $(A+B+C)'$
→ A, B in series with C in parallel $(A \cdot B + C)'$

Bilal Register

Date: / /

RTL → Series • and then complement
Parallel +



E_1	E_2	E_3	V_o
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Suppose E_3, to turn on F.B N → 0.
current flows from supply to gnd.
o/p connected to gnd
Similarly for any diode.
R.B of all I/Ps are 1. → o/c → the I/P voltage appears at o/p
Ground is just → no closed path
↳ no voltage drop

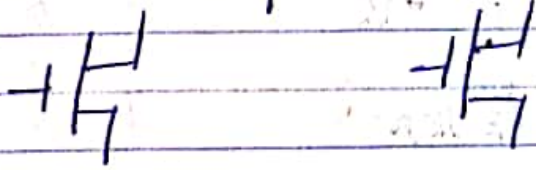
Date: / /

CMOS Logical Family

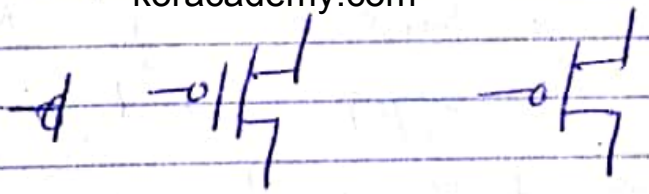
CMOS uses both NMOS and PMOS connected in complementary fashion.

NMOS

NMOS is like an npn transistor.
High → ON → short circuit
Low → OFF → open circuit.

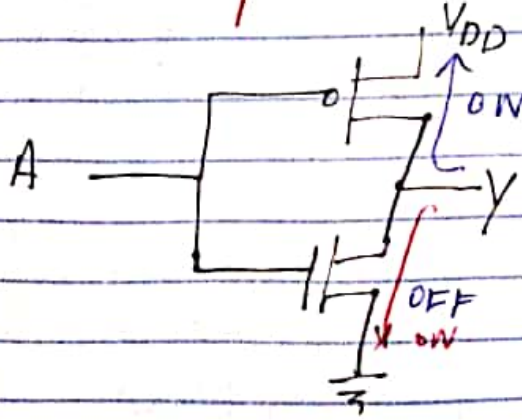


PMOS works in the opposite way. ie
Low → ON → SC
High → OFF → OC



NMOS works on logic high
PMOS

NMOS operates on logic high.
PMOS operates on logic low.

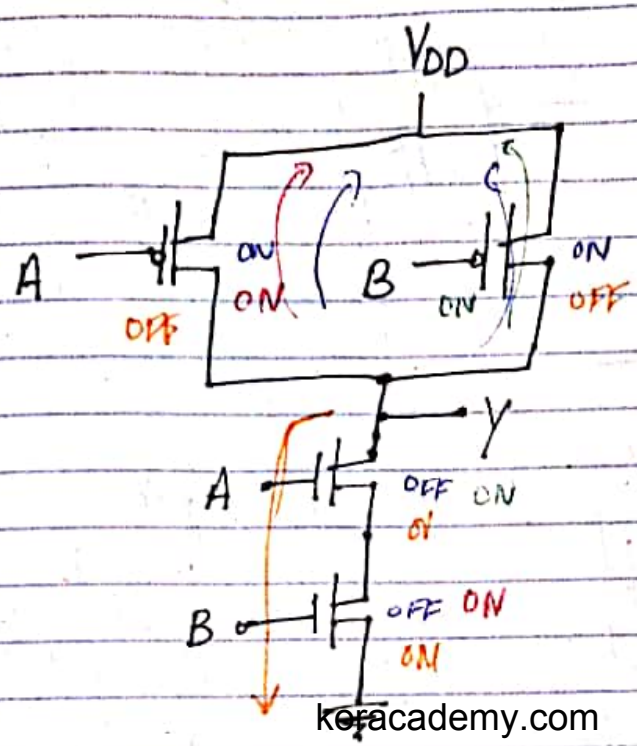


A	Y
L	H
H	L

CMOS inverter / NOT gate

Date: __/__/__

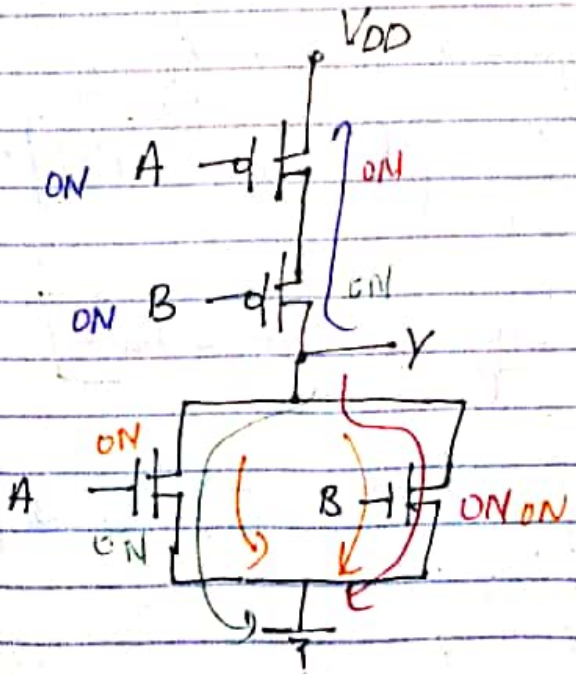
Complementary If NMOS are connected in series, PMOS has to be connected in parallel and vice versa.



A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

This is a CMOS NAND gate.

Advantage of complementary. If o/p is not connected to ground, it is definetly connected to V_{DD} and vice versa.



A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

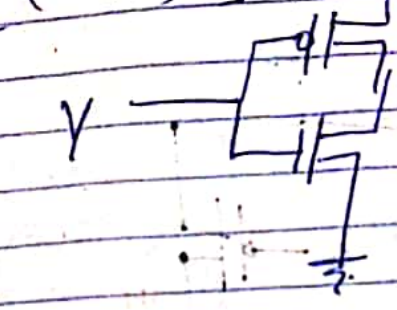
This is a CMOS NOR gate

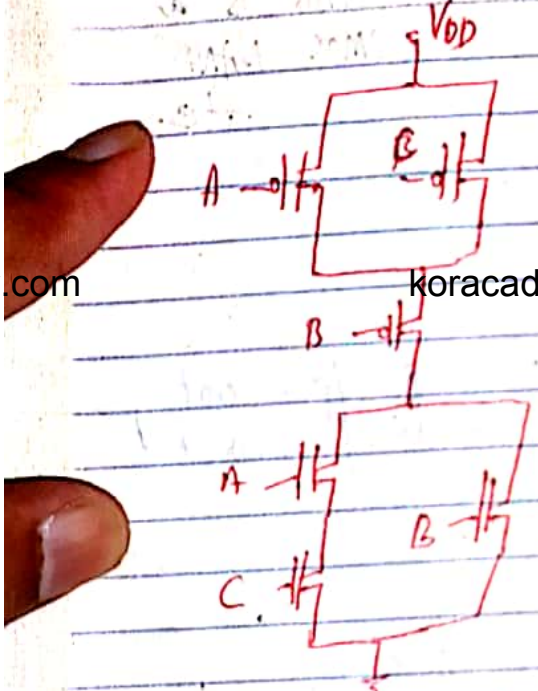
Bilal Register

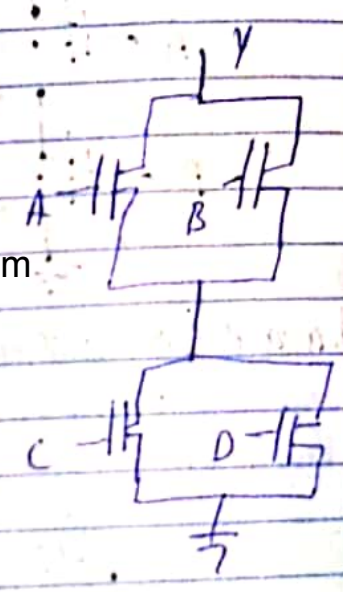
Date: __/__/__

To convert the NOR gate into a OR gate → connect output Y to an inverter

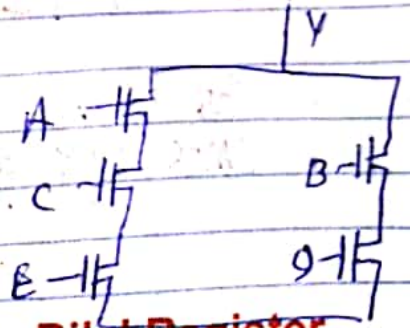
$[(A+B)']' = A+B$





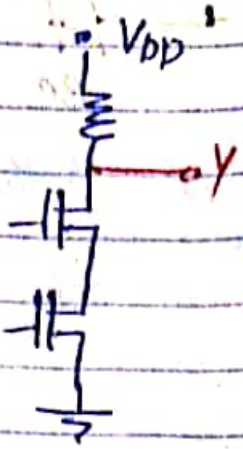


For expression only see NMOS part



Bilal Register

If we talk about NMOS logic family, we put PMOS as a resistor



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

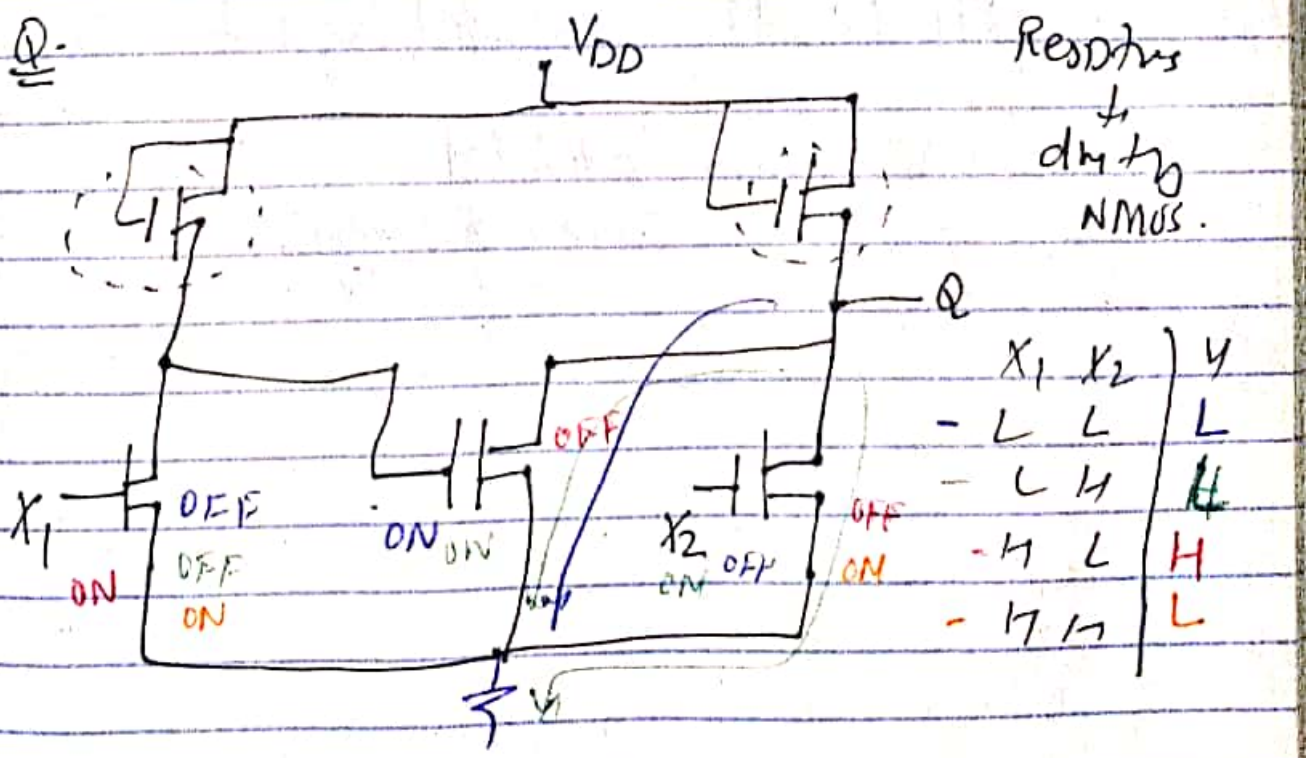
CMOS requires very less area for fabrication

↳ But using resistor require a large silicon surface area → undesirable

→ this will act as a resistor.

↳ So we changed from CMOS to NMOS.

Q.

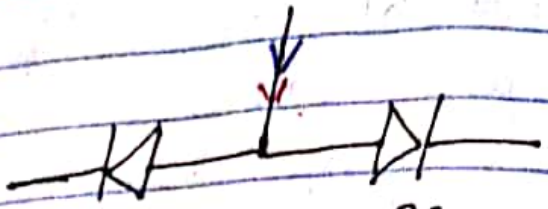


X1	X2	Y
L	L	L
L	H	H
H	L	H
H	H	L

Date: / /

Transistor

NPN



BE

Forward grand F.B

so all curr to left

N → high R.B

no flow of curr

ON.

Reverse ON

BC

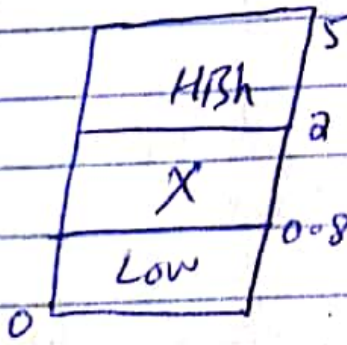
R.B

F.B

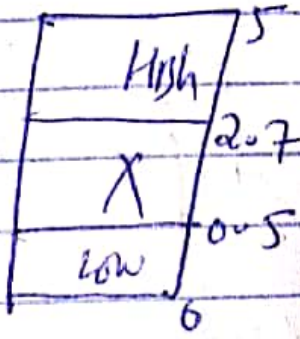
→ all curr flow

TTL

Input window



o/p window



RTL, DTL, TTL → saturated logic families

ECL → non saturated.

↳ in active region.